


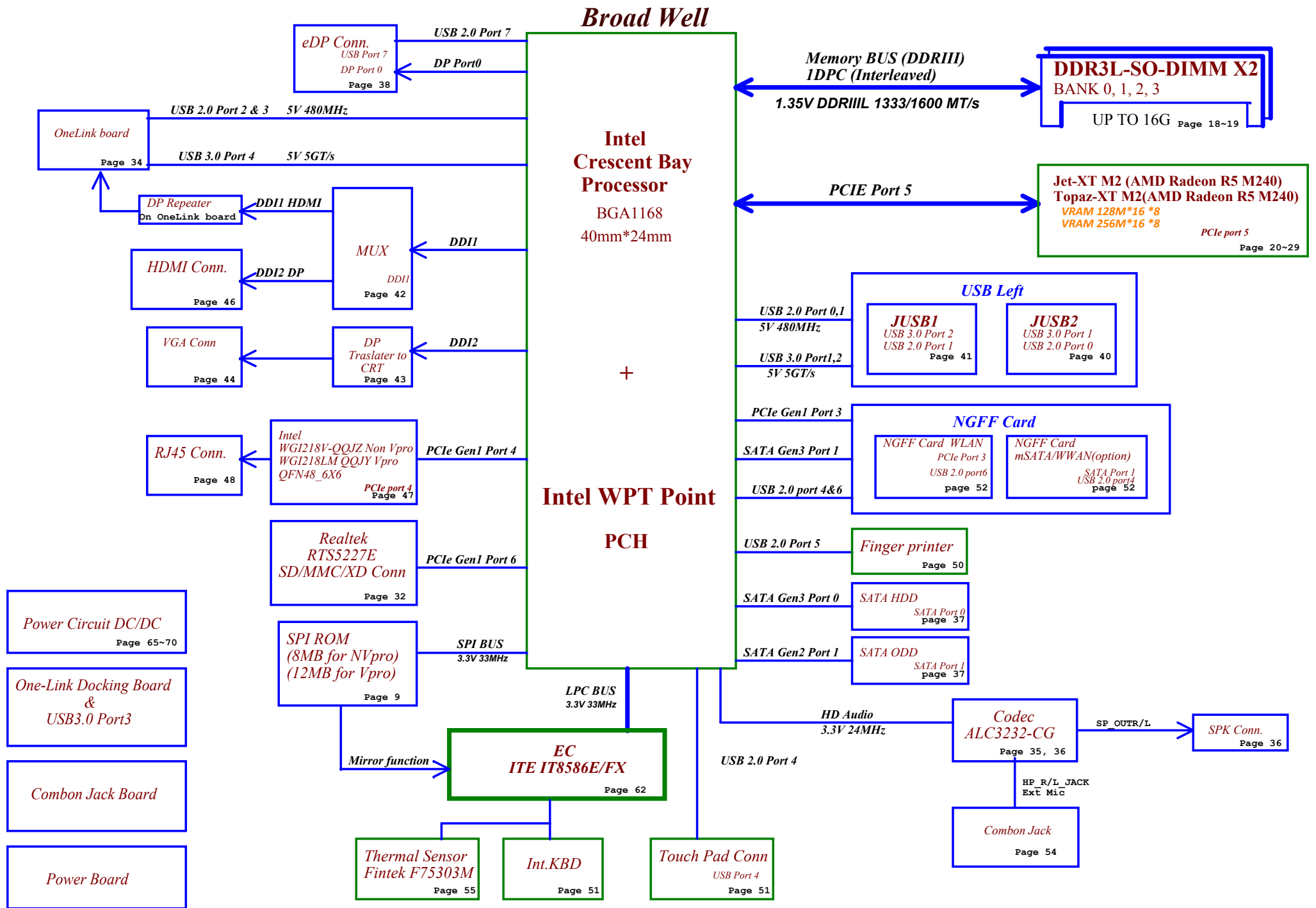
LCFC Confidential

NM-A221 Rev1.0 Schematic

*Intel Crescent Bay Processor with DDRIII + Wild Cat Point PCH
AMD Opal-XT/ Jet-XT*

2013-09-07 Rev1.0

Security Classification	LC Future Center Secret Data			Title		
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Voltage Rails (O --> Means ON , X --> Means OFF)

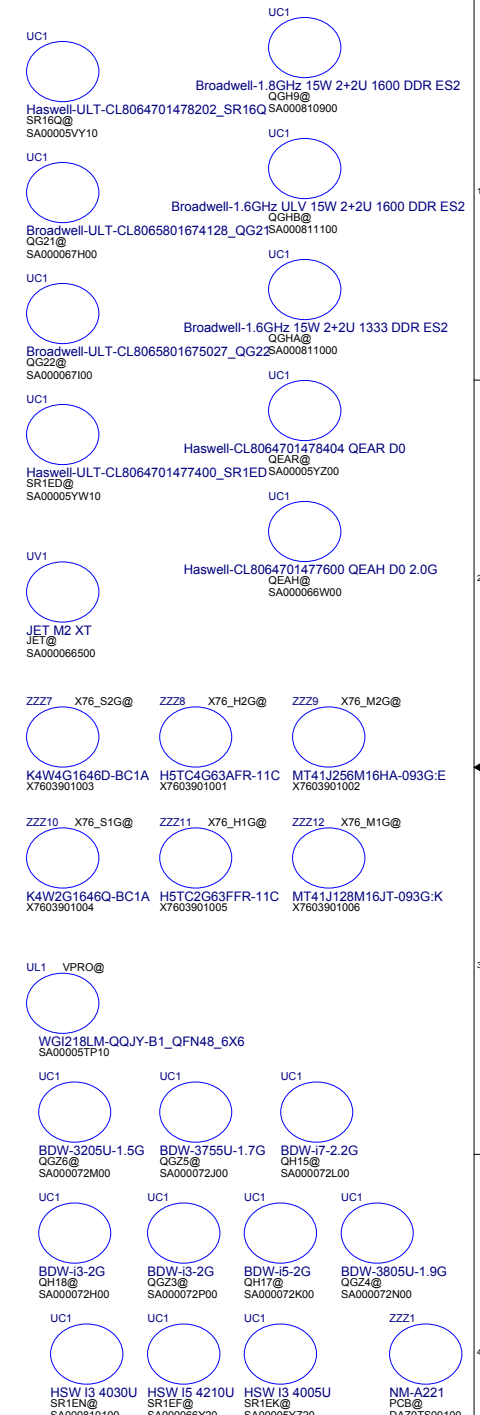
Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

High Speed I/O port

I/O	High Speed Signal	Configuration	Port assignment
1	USB3 1	USB3 1	On MB USB
2	USB3 2	USB3 2	On MB USB
3	PCIE 1 / USB3 3	NC	NC
4	PCIE 2 / USB3 4	USB3 4	Docking USB
5	PCIE 3	PCIE 3	WLAN
6	PCIE 4	PCIE 4	LAN
7	PCIE 5 L0	PCIE 5 L0	GPU
8	PCIE 5 L1	PCIE 5 L1	GPU
9	PCIE 5 L2	PCIE 5 L2	GPU
10	PCIE 5 L3	PCIE 5 L3	GPU
11	PCIE 6 L0 / SATA 3	PCIE 6	Cardreader
12	PCIE 6 L1 / SATA 2	SATA 2	mSATA
13	PCIE 6 L2 / SATA 1	SATA 1	ODD
14	PCIE 6 L3 / SATA 0	SATA 0	HDD

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function (Option with TS@)
TPM@	Trusted Platform Module (TPM)
NM14@	14" SKU ID
NM15@	15" SKU ID
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
X76@	GPU VRAM Setting
M2G@	Micron 256Mx16 VRAM
M1G@	Micron 128Mx16 VRAM
S2G@	Samsung 256Mx16 VRAM
S1G@	Samsung 128Mx16 VRAM
ME@	ME Connector
TS@	Touch screen function
DEBUG@	For debug
BYPASS@	For bypass
MIRROR@	For mirror function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
X76_S2G@	For Samsung 2G VRAM



SMBUS Control Table

	SOURCE	Main VGA	LAN	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	CP Module	Charger
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	V +3V_PCH	X	X	X	X	X	X	X	X
PCH_SML1CLK PCH_SML1DATA	PCH +3V_PCH	V +3VS	X	X	V +3VS	X	X	V +3VS	X	X	X
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	X	V +3VL	X	X	X	X	X	X	V +3VL
PCH_SMBCLK PCH_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	X	X	V +3V_PCH	V +3VS	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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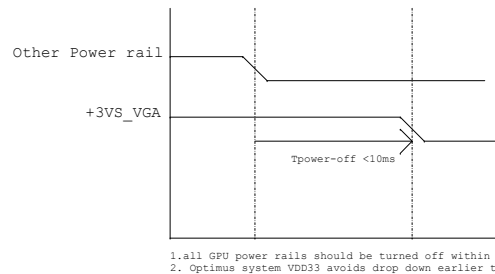
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[illegible]

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

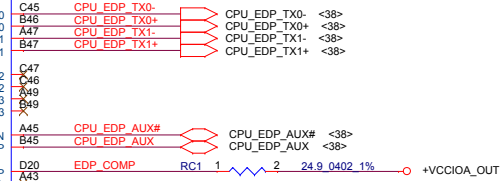
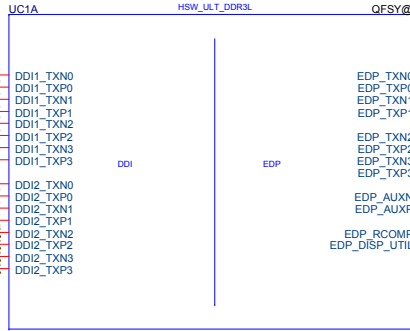
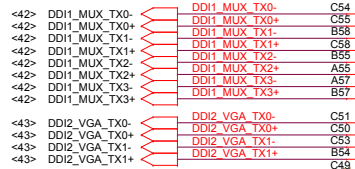
GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

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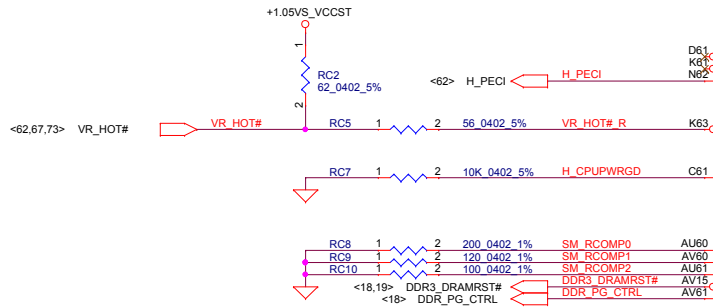
For 14" : DOCKING
For 15" : HDMI & DOCKING

For 14" : HDMI
For 15" : VGA

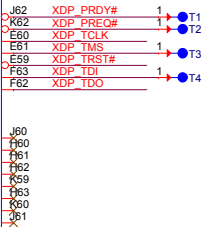
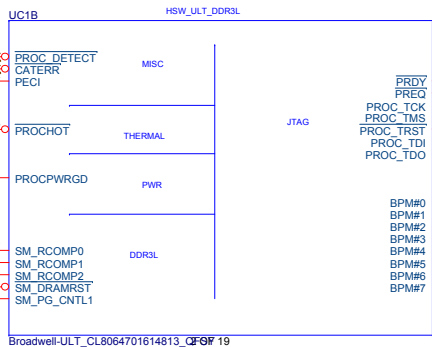


EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC25 close to MCP
Trace Width=20mil, Spacing=25mil, Max length=100mil

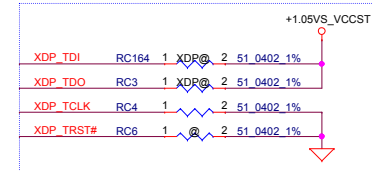
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Broadwell-ULT_CL8064701614813_QFSY
SA000064600



DDR3 COMPENSATION SIGNALS
1. Trace width=12~15 mil, Spcing=20 mils,
Max trace length= 500 mil,
2. All of R Close to MCP



PU/PD Res. For CPU-XDP SIGNAL, Place R Closer to CPU



XDP PU/PD portion need to check again.

Interleaved (Butterfly Topology)
Broadwell Platform System Memory Interface
Document Number: 528378
BDW U DDR3L/DDR3L-RS SO-DIMM Interleaved Recommendations

Channel A Byte 0 & 1

Channel B Byte 0 & 1

Channel A Byte 2 & 3

Channel B Byte 2 & 3

MCP
Channel A

Channel A Byte 4 & 5

Channel B Byte 4 & 5

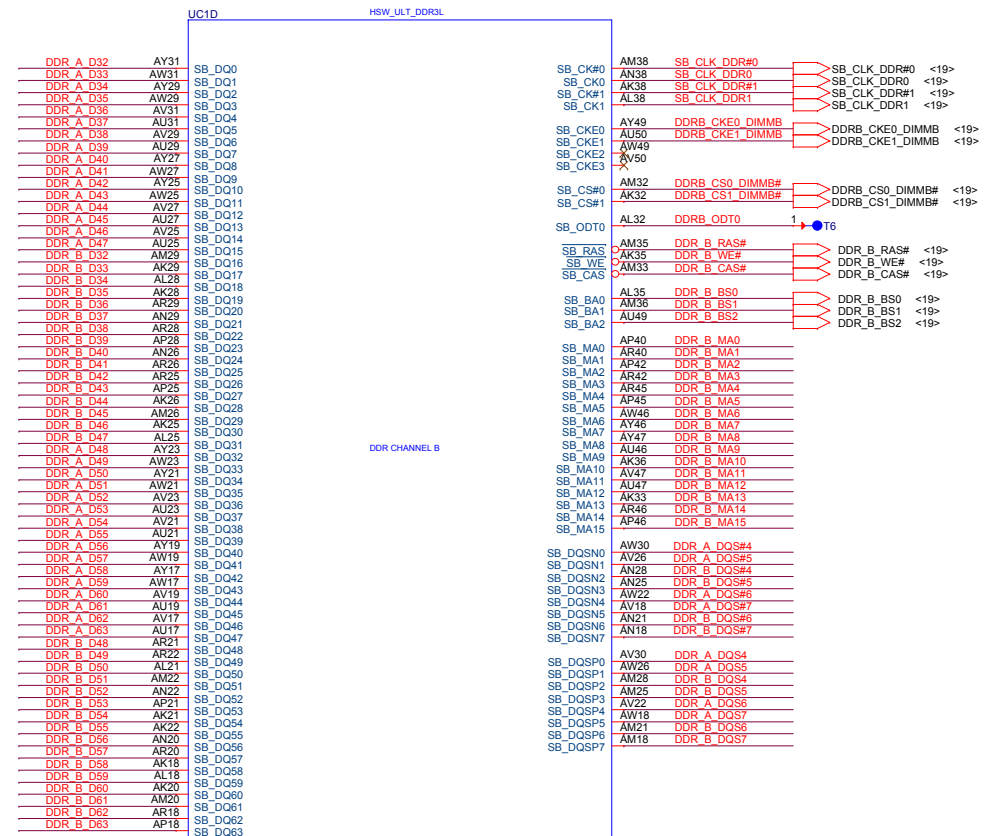
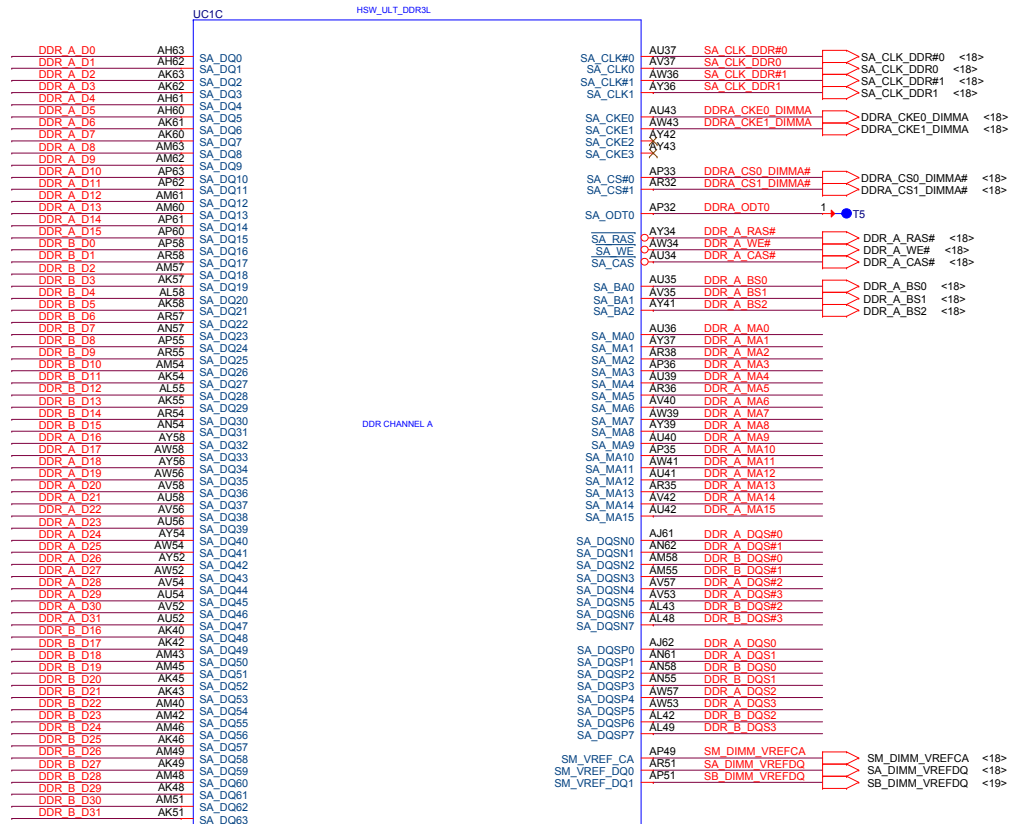
Channel A Byte 6 & 7

Channel B Byte 6 & 7

MCP
Channel B

<18> DDR_A_D[0..63]
<18> DDR_A_DQS[0..7]
<18> DDR_A_DQS[0..7]
<18> DDR_A_MA[0..15]

<19> DDR_B_D[0..63]
<19> DDR_B_DQS[0..7]
<19> DDR_B_DQS[0..7]
<19> DDR_B_MA[0..15]



Broadwell-ULT_CL8064701614813_QF0F 19

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+RTCBATT

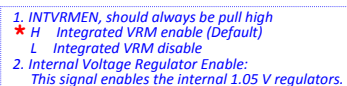
RC11 1 2 0.0402 5%


+RTCVCC

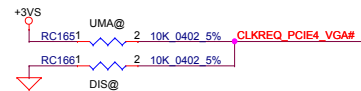
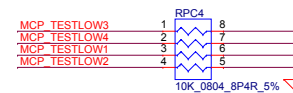
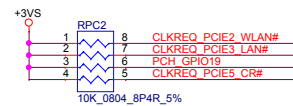
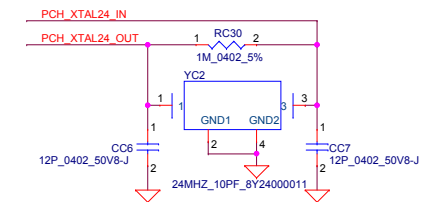
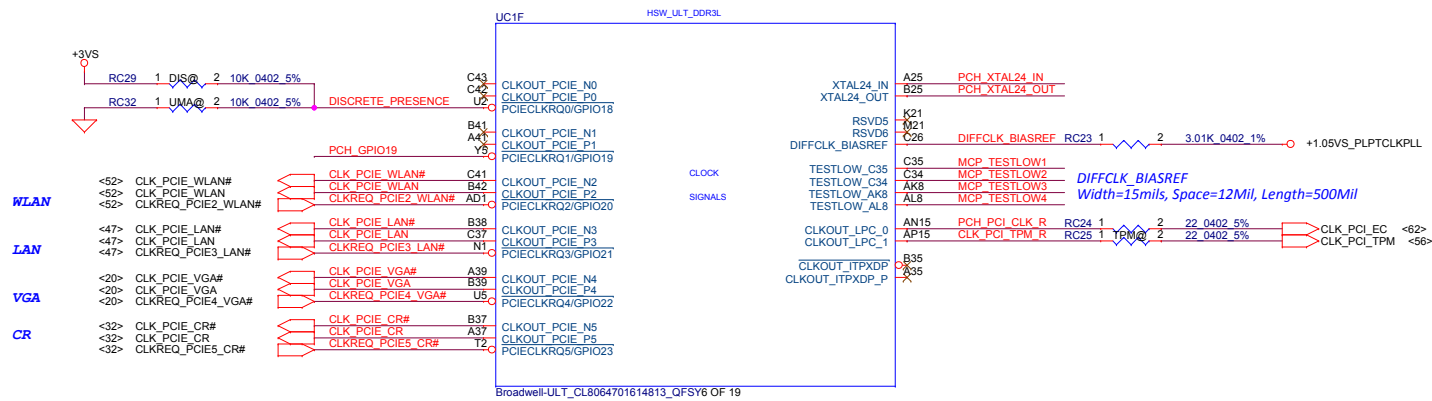
CC2 1 2 1u_0402_10V6-K

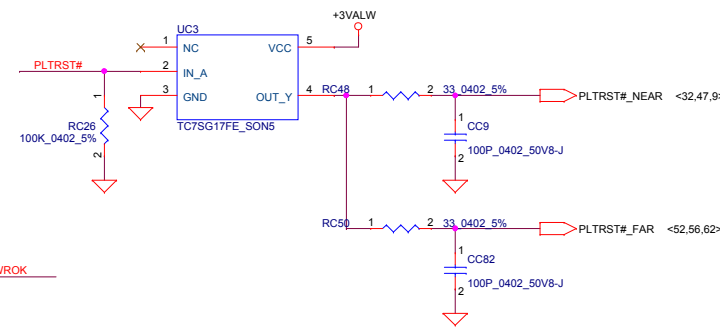
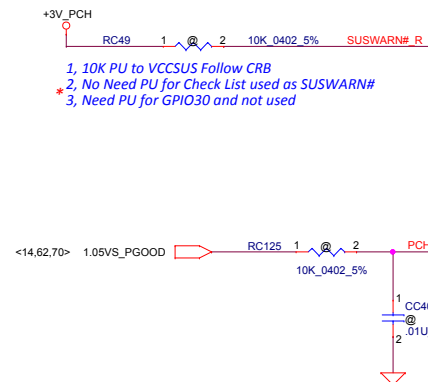
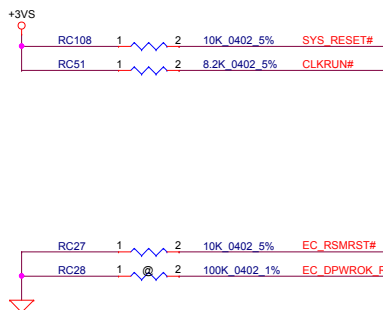
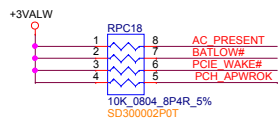
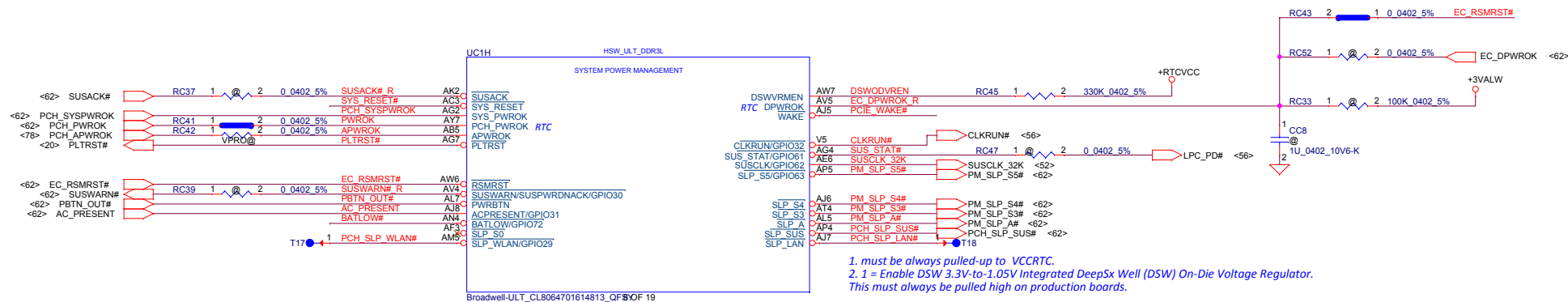
+RTCBATT, +RTCVCC
Trace width = 20mils

1. Space > 15mils
2. No trace under crystal
3. No trace on opposite side of MCP for temp influence



Title		RTC/HDA/SATA/PCle/JTAG 	
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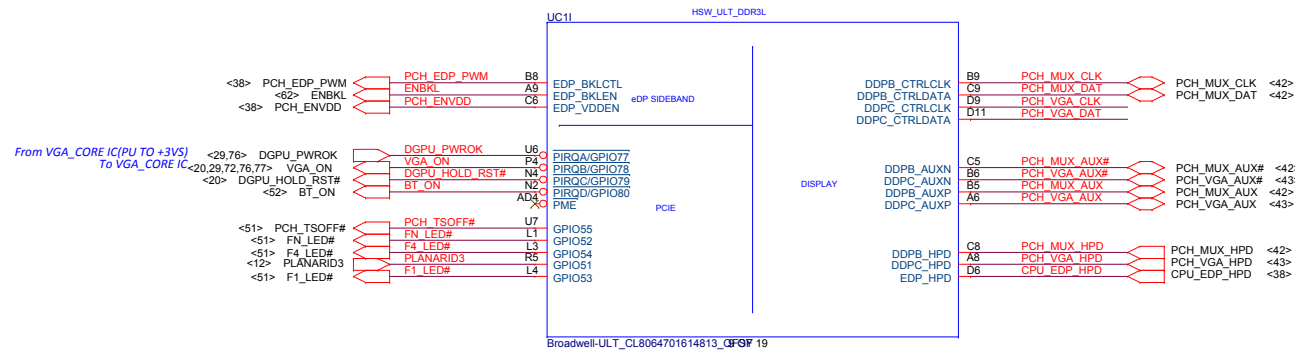




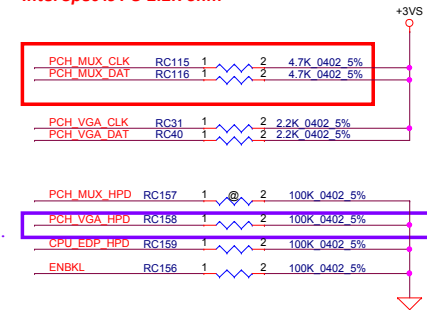
SUSWARN#_R 1 RC109 2 SUSACK#_R 0_0402_5% SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

APWROK 1 RC111 2 PWRK# 0_0402_5% For platforms not supporting IntelR AMT it can be connected to PWRK#.

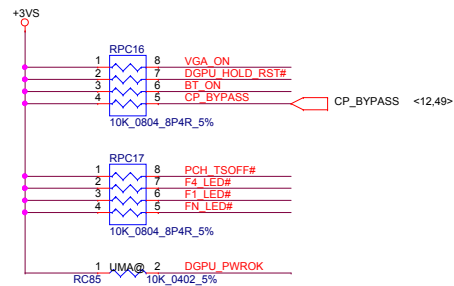
This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state. RSMRST# <--> DPWROK



1. **VENDOR 紙板PU** , 紙板Vih anf Vil Tmeet SPEC value.
2. Vender fine tune recommend value.(Pass Through Mode)
3. Vendor recommend use PU 4.7K ohm. (10/1) Intel Spec is PU 2.2K ohm



After testing, check if can un-stuff.



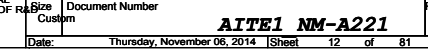
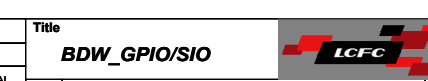
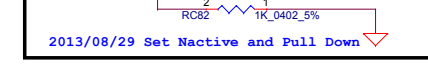
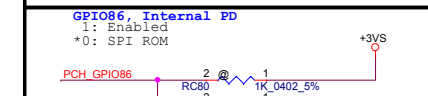
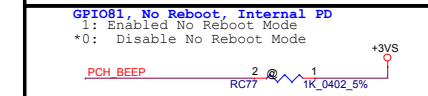
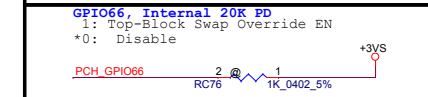
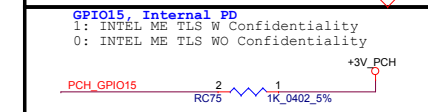
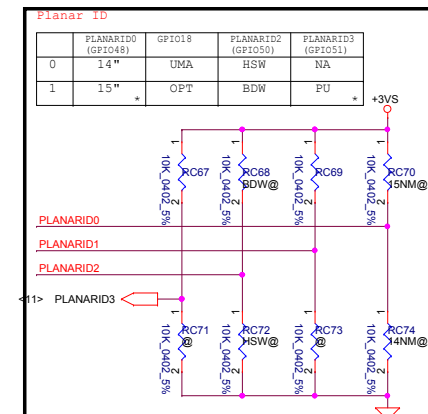
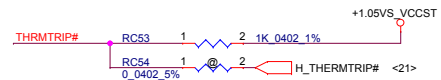
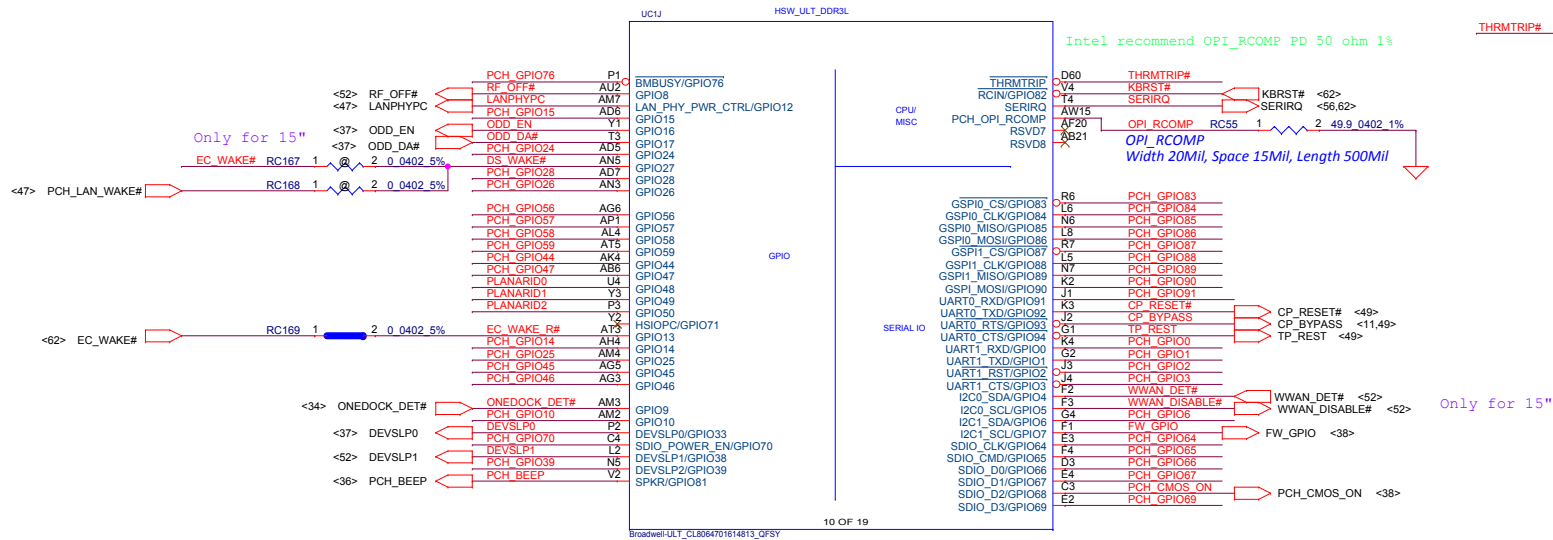
DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected

* 1: Port B or C is detected
0: Port B or C is not detected

Internal PD 15K~40K, nominal 20K

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GPU

WLAN

LAN

3D CCD

DOCKNG

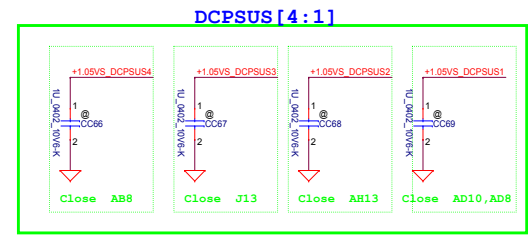
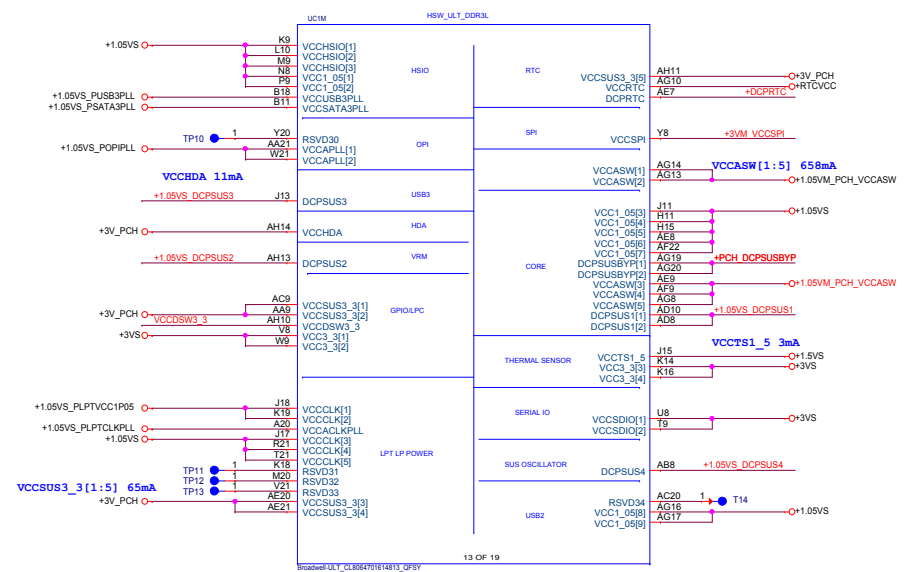
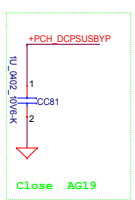
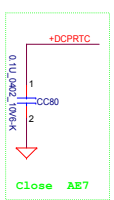
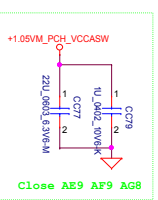
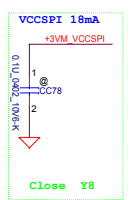
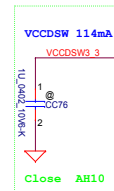
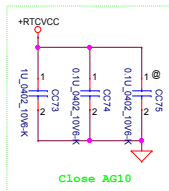
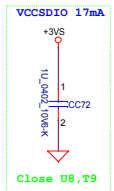
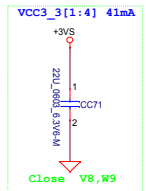
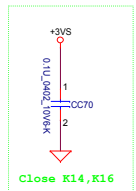
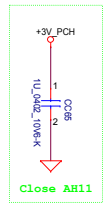
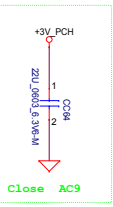
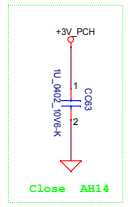
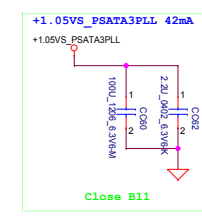
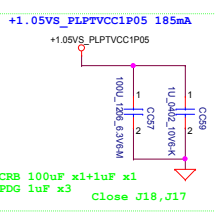
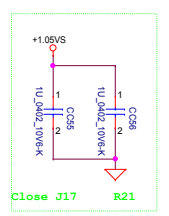
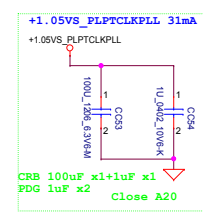
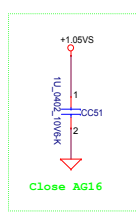
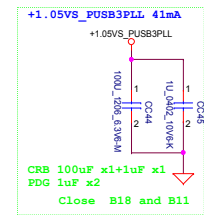
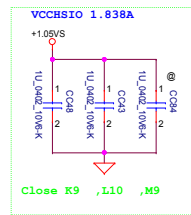
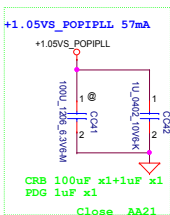
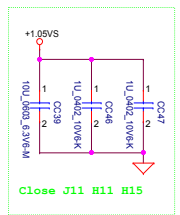
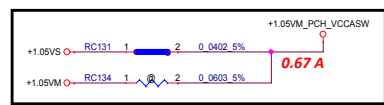
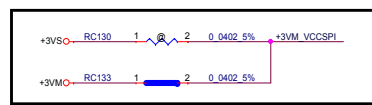
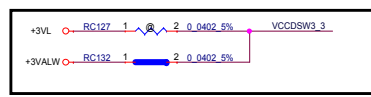
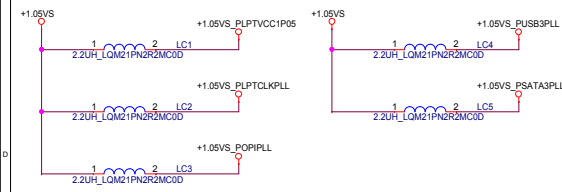
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Haswell MCP (VSS)

UC1N HSW_ULT_DDR3L

UC1O HSW_ULT_DDR3L

UC1P HSW_ULT_DDR3L

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VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128

AJ35 AJ36 AJ37 AJ38 AJ39 AJ40 AJ41 AJ42 AJ43 AJ44 AJ45 AJ46 AJ47 AJ48 AJ49 AJ50 AJ51 AJ52 AJ53 AJ54 AJ55 AJ56 AJ57 AJ58 AJ59 AJ60 AJ61 AJ62 AJ63 AJ64 AJ65 AJ66 AJ67 AJ68 AJ69 AJ70 AJ71 AJ72 AJ73 AJ74 AJ75 AJ76 AJ77 AJ78 AJ79 AJ80 AJ81 AJ82 AJ83 AJ84 AJ85 AJ86 AJ87 AJ88 AJ89 AJ90 AJ91 AJ92 AJ93 AJ94 AJ95 AJ96 AJ97 AJ98 AJ99 AJ100

AP22 AP23 AP24 AP25 AP26 AP27 AP28 AP29 AP30 AP31 AP32 AP33 AP34 AP35 AP36 AP37 AP38 AP39 AP40 AP41 AP42 AP43 AP44 AP45 AP46 AP47 AP48 AP49 AP50 AP51 AP52 AP53 AP54 AP55 AP56 AP57 AP58 AP59 AP60 AP61 AP62 AP63 AP64 AP65 AP66 AP67 AP68 AP69 AP70 AP71 AP72 AP73 AP74 AP75 AP76 AP77 AP78 AP79 AP80 AP81 AP82 AP83 AP84 AP85 AP86 AP87 AP88 AP89 AP90 AP91 AP92 AP93 AP94 AP95 AP96 AP97 AP98 AP99 AP100

AV59 AV60 AV61 AV62 AV63 AV64 AV65 AV66 AV67 AV68 AV69 AV70 AV71 AV72 AV73 AV74 AV75 AV76 AV77 AV78 AV79 AV80 AV81 AV82 AV83 AV84 AV85 AV86 AV87 AV88 AV89 AV90 AV91 AV92 AV93 AV94 AV95 AV96 AV97 AV98 AV99 AV100

D33 D34 D35 D36 D37 D38 D39 D40 D41 D42 D43 D44 D45 D46 D47 D48 D49 D50 D51 D52 D53 D54 D55 D56 D57 D58 D59 D60 D61 D62 D63 D64 D65 D66 D67 D68 D69 D70 D71 D72 D73 D74 D75 D76 D77 D78 D79 D80 D81 D82 D83 D84 D85 D86 D87 D88 D89 D90 D91 D92 D93 D94 D95 D96 D97 D98 D99 D100

VSS257 VSS258 VSS259 VSS260 VSS261 VSS262 VSS263 VSS264 VSS265 VSS266 VSS267 VSS268 VSS269 VSS270 VSS271 VSS272 VSS273 VSS274 VSS275 VSS276 VSS277 VSS278 VSS279 VSS280 VSS281 VSS282 VSS283 VSS284 VSS285 VSS286 VSS287 VSS288 VSS289 VSS290 VSS291 VSS292 VSS293 VSS294 VSS295 VSS296 VSS297 VSS298 VSS299

H17 H18 H19 H20 H21 H22 H23 H24 H25 H26 H27 H28 H29 H30 H31 H32 H33 H34 H35 H36 H37 H38 H39 H40 H41 H42 H43 H44 H45 H46 H47 H48 H49 H50 H51 H52 H53 H54 H55 H56 H57 H58 H59 H60 H61 H62 H63 H64 H65 H66 H67 H68 H69 H70 H71 H72 H73 H74 H75 H76 H77 H78 H79 H80 H81 H82 H83 H84 H85 H86 H87 H88 H89 H90 H91 H92 H93 H94 H95 H96 H97 H98 H99 H100

VSS300 VSS301 VSS302 VSS303 VSS304 VSS305 VSS306 VSS307 VSS308 VSS309 VSS310 VSS311 VSS312 VSS313 VSS314 VSS315 VSS316 VSS317 VSS318 VSS319 VSS320 VSS321 VSS322 VSS323 VSS324 VSS325 VSS326 VSS327 VSS328 VSS329 VSS330 VSS331 VSS332 VSS333 VSS334 VSS335 VSS336 VSS337

V58 AH46 V23 V33 AH16

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RC143 100_0402_1%

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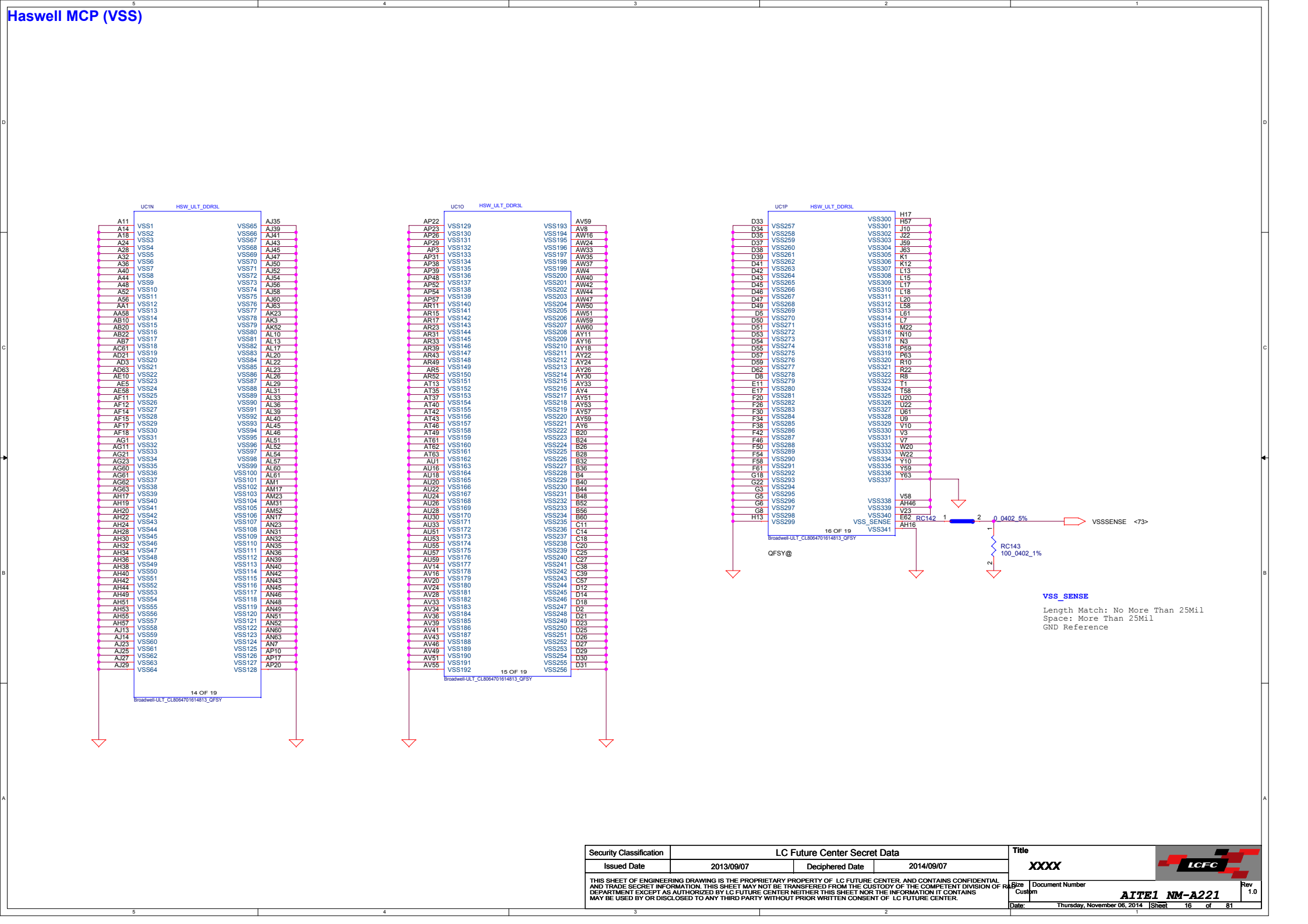
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Haswell MCP (VSS)

UC1N HSW_ULT_DDR3L

UC1O HSW_ULT_DDR3L

UC1P HSW_ULT_DDR3L

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VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128

AJ35 AJ36 AJ37 AJ38 AJ39 AJ40 AJ41 AJ42 AJ43 AJ44 AJ45 AJ46 AJ47 AJ48 AJ49 AJ50 AJ51 AJ52 AJ53 AJ54 AJ55 AJ56 AJ57 AJ58 AJ59 AJ60 AJ61 AJ62 AJ63 AJ64 AJ65 AJ66 AJ67 AJ68 AJ69 AJ70 AJ71 AJ72 AJ73 AJ74 AJ75 AJ76 AJ77 AJ78 AJ79 AJ80 AJ81 AJ82 AJ83 AJ84 AJ85 AJ86 AJ87 AJ88 AJ89 AJ90 AJ91 AJ92 AJ93 AJ94 AJ95 AJ96 AJ97 AJ98 AJ99 AP20 AP21

AP22 AP23 AP24 AP25 AP26 AP27 AP28 AP29 AP30 AP31 AP32 AP33 AP34 AP35 AP36 AP37 AP38 AP39 AP40 AP41 AP42 AP43 AP44 AP45 AP46 AP47 AP48 AP49 AP50 AP51 AP52 AP53 AP54 AP55 AP56 AP57 AP58 AP59 AP60 AP61 AP62 AP63 AP64 AP65 AP66 AP67 AP68 AP69 AP70 AP71 AP72 AP73 AP74 AP75 AP76 AP77 AP78 AP79 AP80 AP81 AP82 AP83 AP84 AP85 AP86 AP87 AP88 AP89 AP90 AP91 AP92 AP93 AP94 AP95 AP96 AP97 AP98 AP99 AV55 AV56

AV59 AV60 AV61 AV62 AV63 AV64 AV65 AV66 AV67 AV68 AV69 AV70 AV71 AV72 AV73 AV74 AV75 AV76 AV77 AV78 AV79 AV80 AV81 AV82 AV83 AV84 AV85 AV86 AV87 AV88 AV89 AV90 AV91 AV92 AV93 AV94 AV95 AV96 AV97 AV98 AV99 D31 D32

D33 D34 D35 D36 D37 D38 D39 D40 D41 D42 D43 D44 D45 D46 D47 D48 D49 D50 D51 D52 D53 D54 D55 D56 D57 D58 D59 D60 D61 D62 D63 D64 D65 D66 D67 D68 D69 D70 D71 D72 D73 D74 D75 D76 D77 D78 D79 D80 D81 D82 D83 D84 D85 D86 D87 D88 D89 D90 D91 D92 D93 D94 D95 D96 D97 D98 D99 VSS299

VSS300 VSS301 VSS302 VSS303 VSS304 VSS305 VSS306 VSS307 VSS308 VSS309 VSS310 VSS311 VSS312 VSS313 VSS314 VSS315 VSS316 VSS317 VSS318 VSS319 VSS320 VSS321 VSS322 VSS323 VSS324 VSS325 VSS326 VSS327 VSS328 VSS329 VSS330 VSS331 VSS332 VSS333 VSS334 VSS335 VSS336 VSS337

V58 AH46 V23 V33 AH16

RC142 1 2 0.0402 5%

RC143 100_0402_1%

VSSSENSE <73>

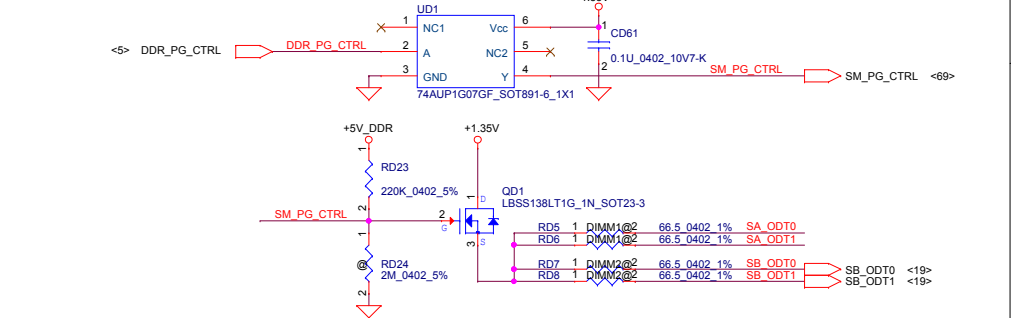
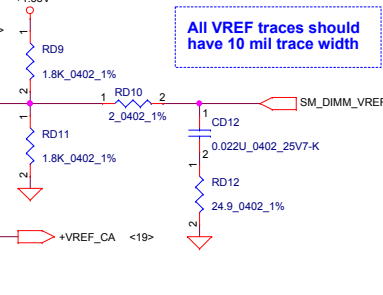
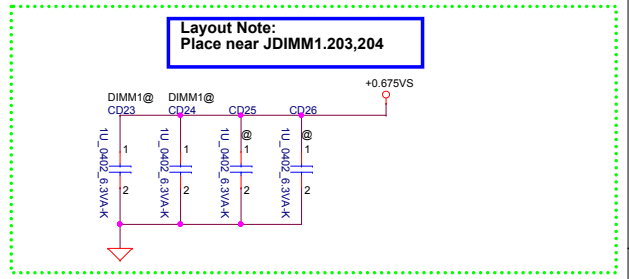
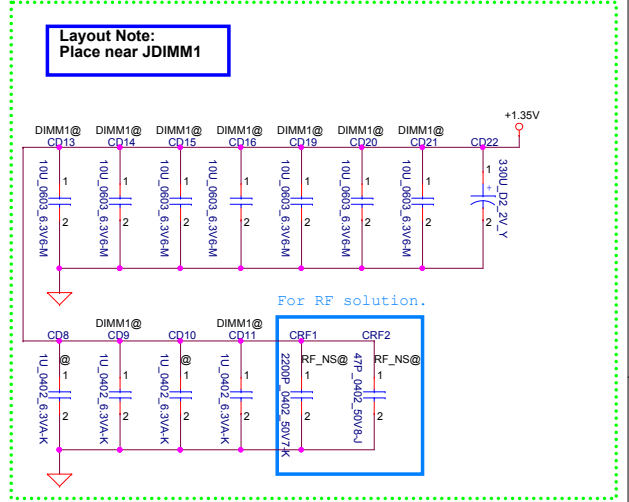
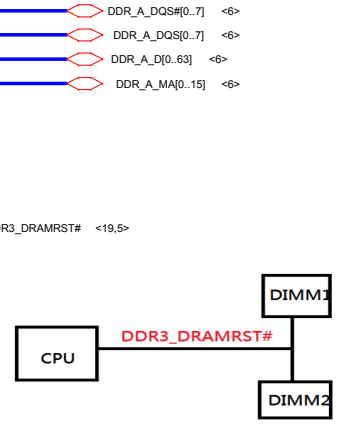
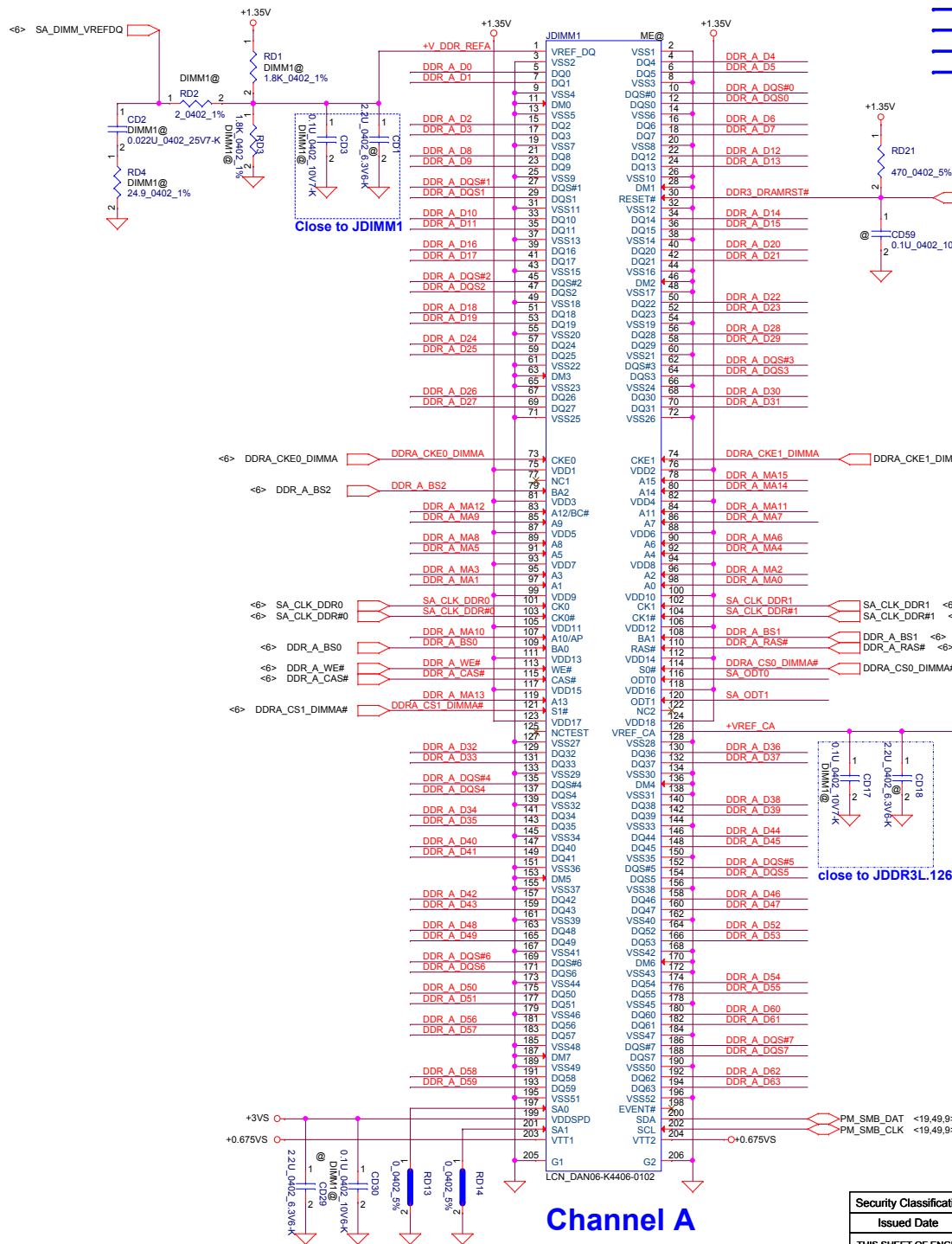
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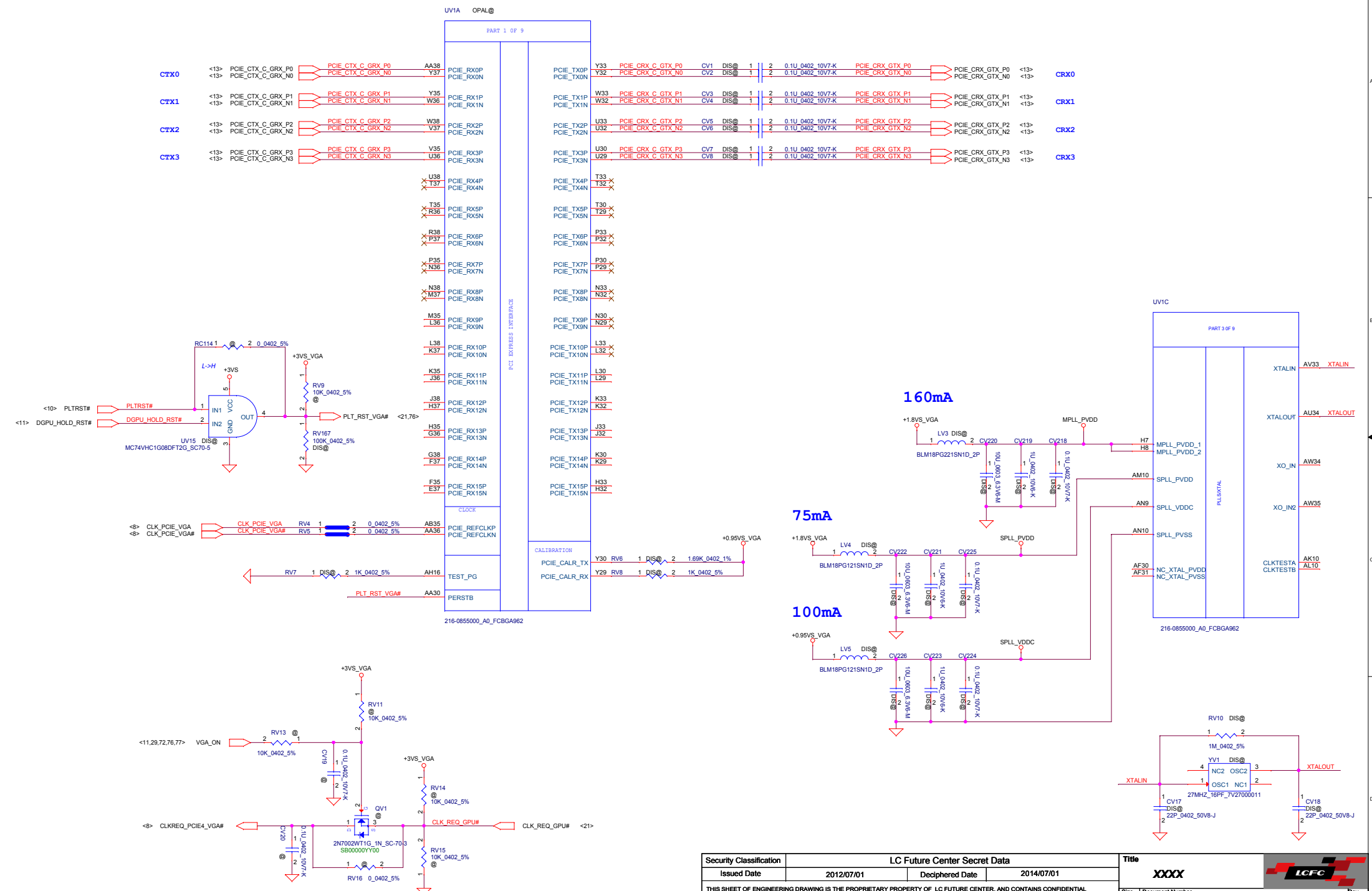
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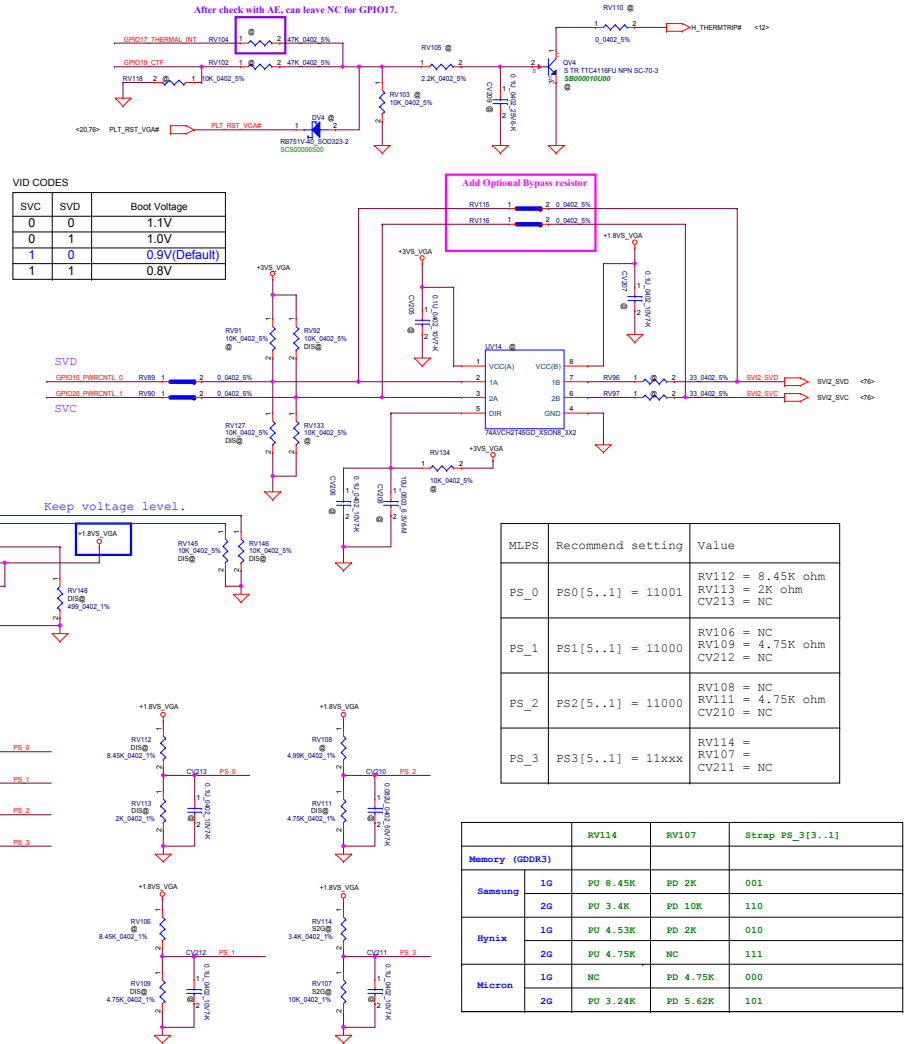
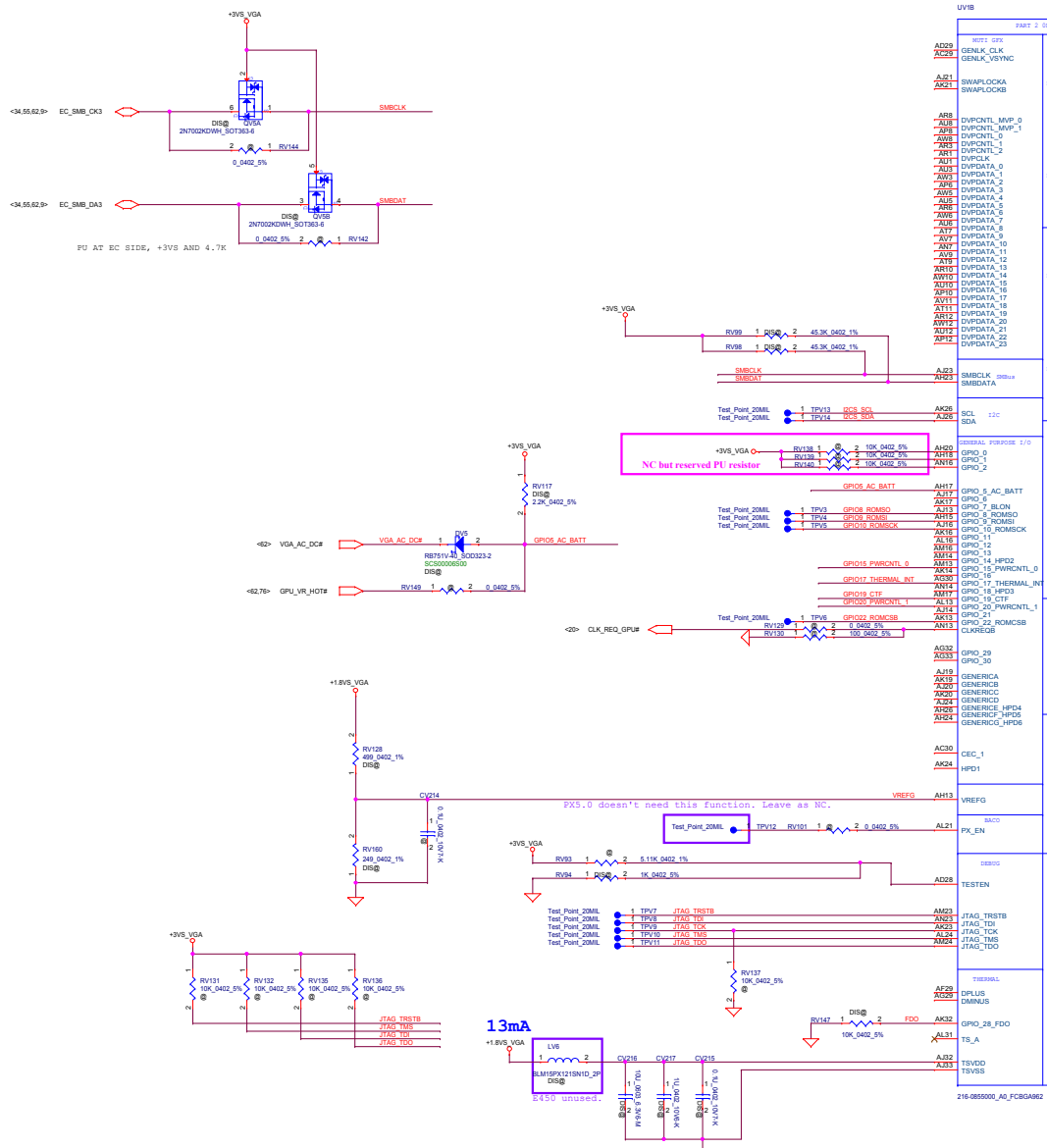
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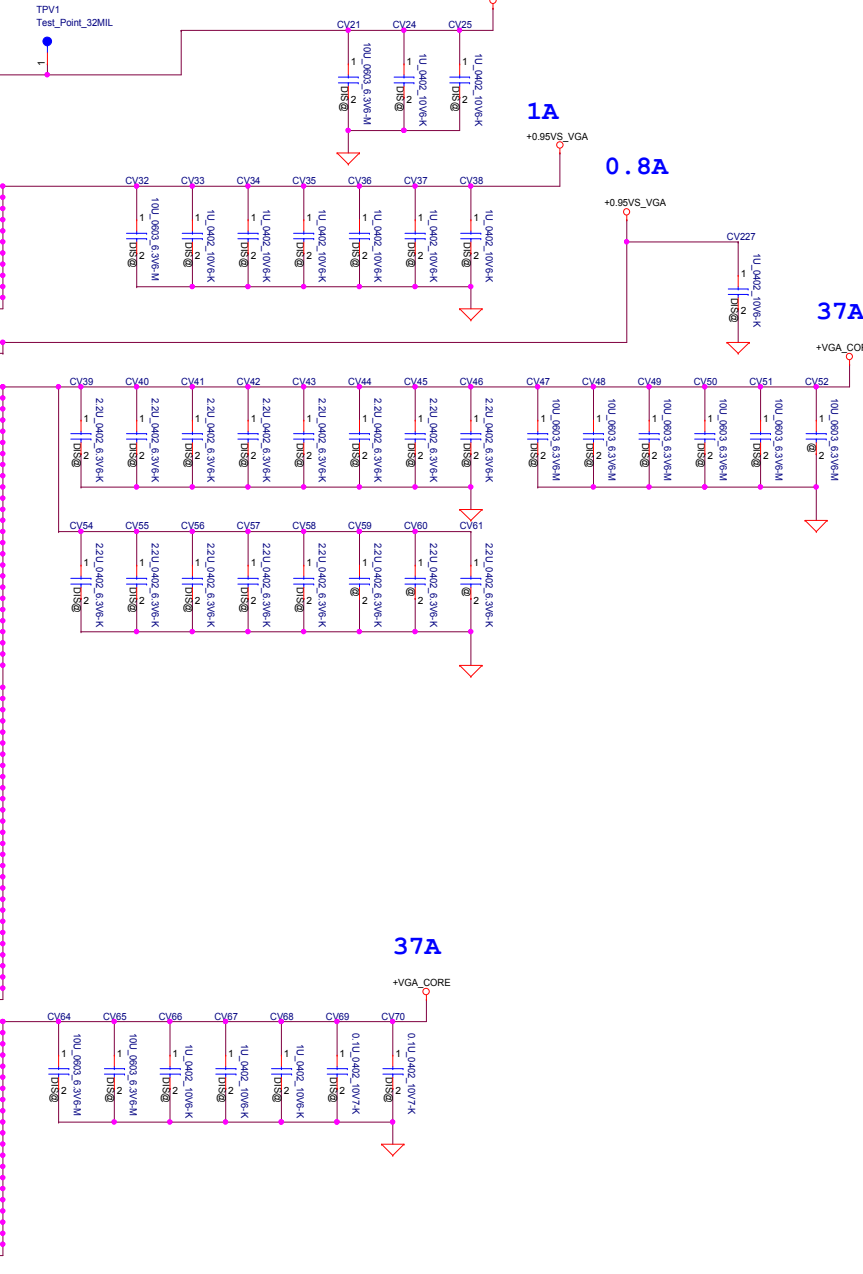
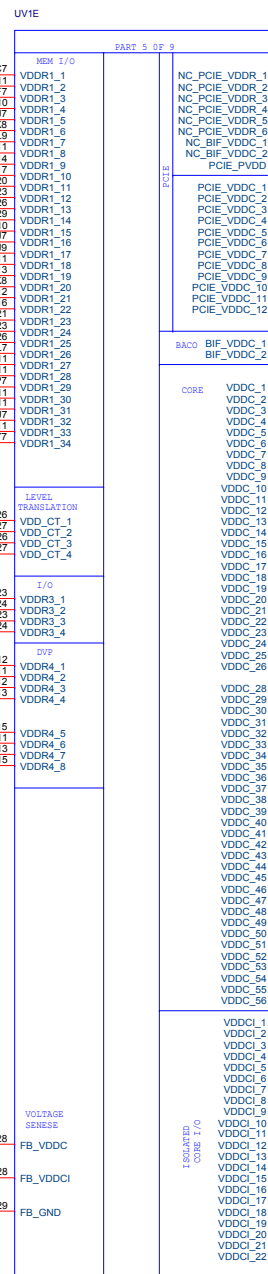
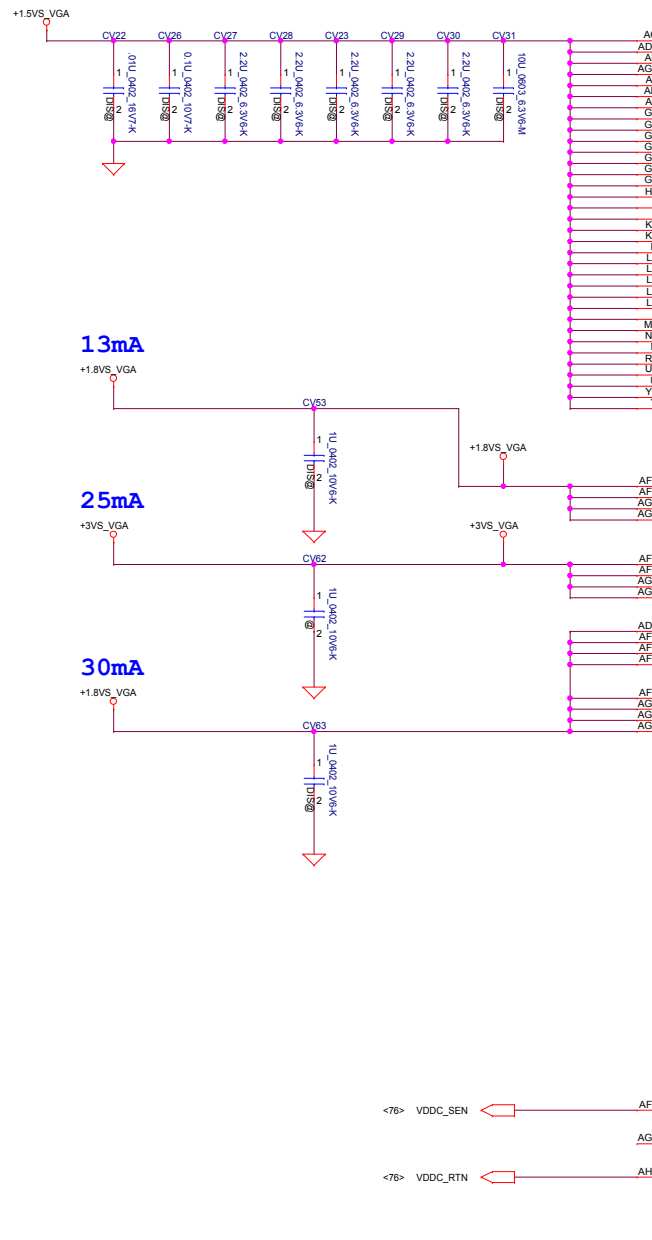



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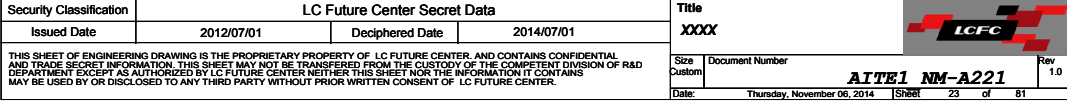
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0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

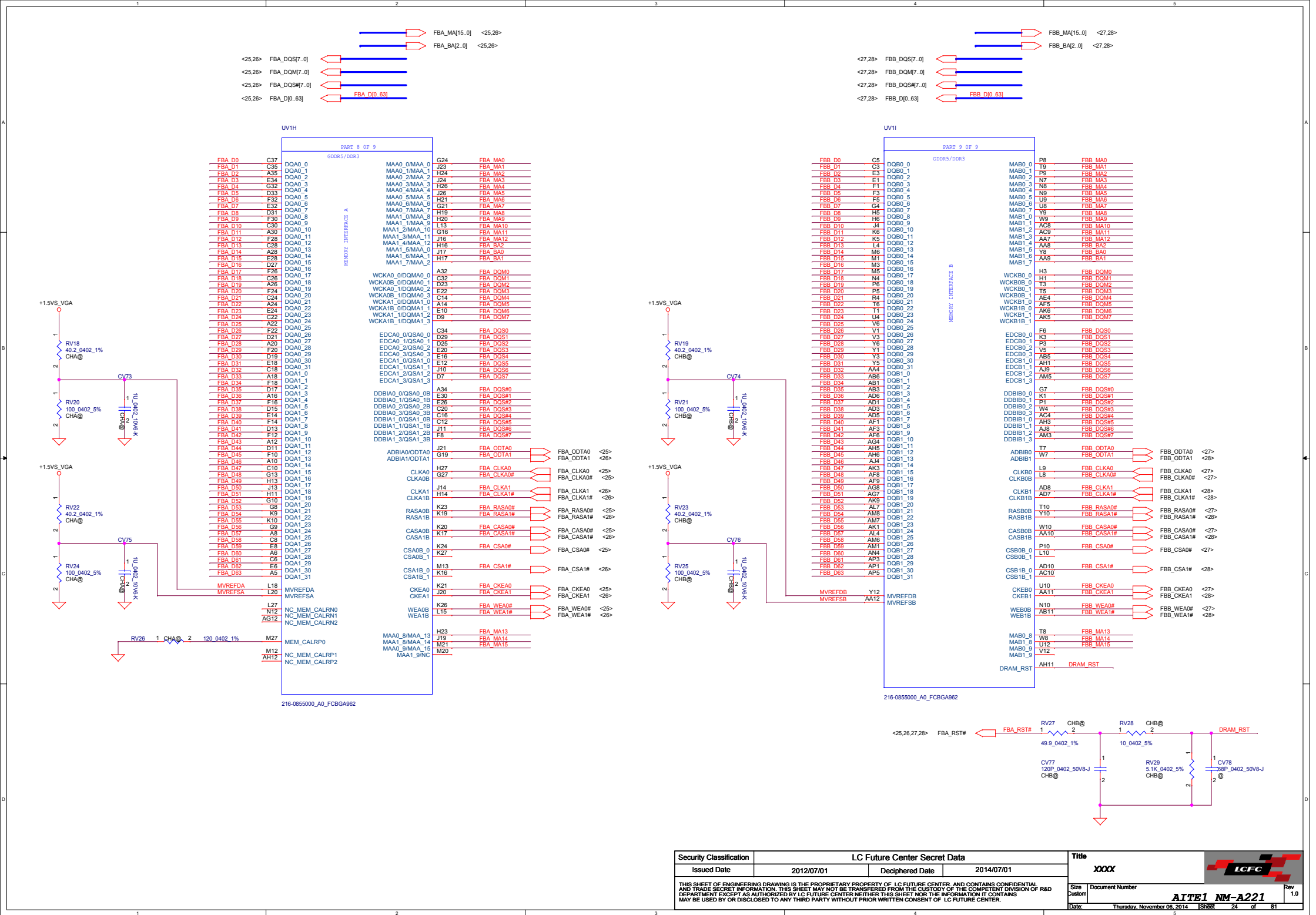
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PS_0	PS0[5..1] = 11001	RV112 = 8.45K ohm RV113 = 2K ohm CV213 = NC
PS_1	PS1[5..1] = 11000	RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2	PS2[5..1] = 11000	RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3	PS3[5..1] = 11xxx	RV114 = NC RV107 = CV211 = NC

	RV114	RV107	Strap PS_3[3..1]
Memory (GDDR3)			
Samsung	1G	PU 8.45K	PD 2K
	2G	PU 3.4K	PD 10K
Bnyx	1G	PU 4.53K	PD 2K
	2G	PU 4.75K	NC
Micron	1G	NC	PD 4.75K
	2G	PU 3.24K	PD 5.62K

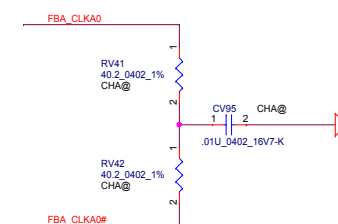
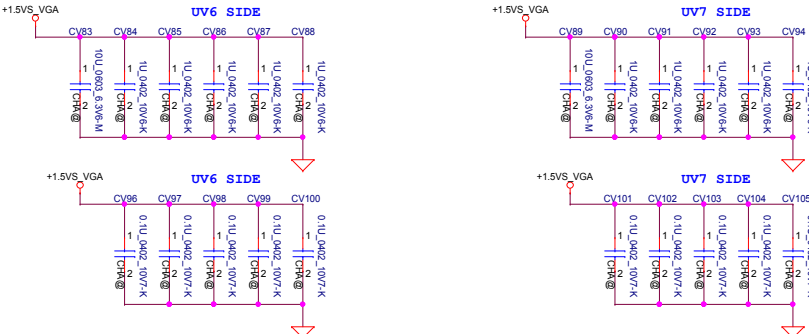
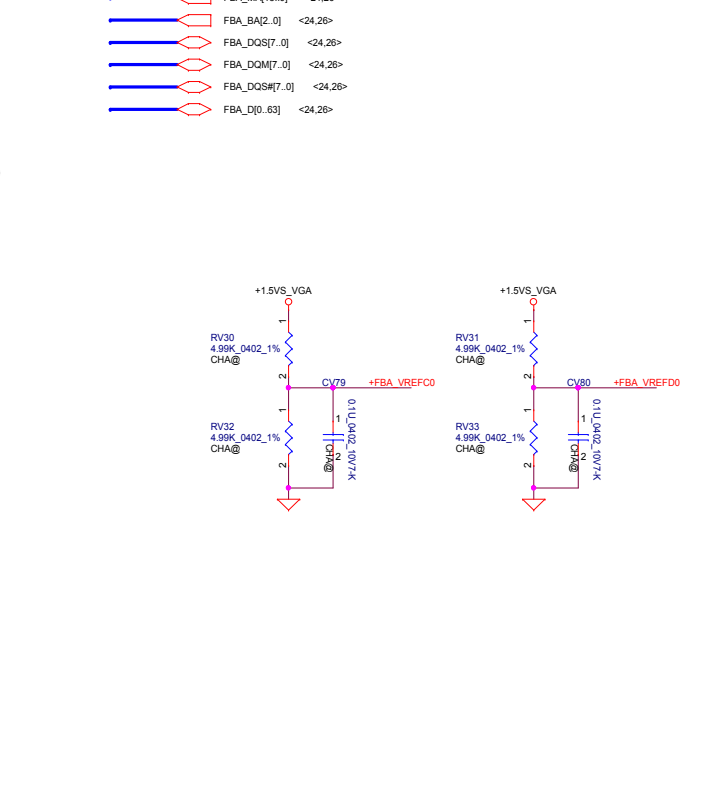
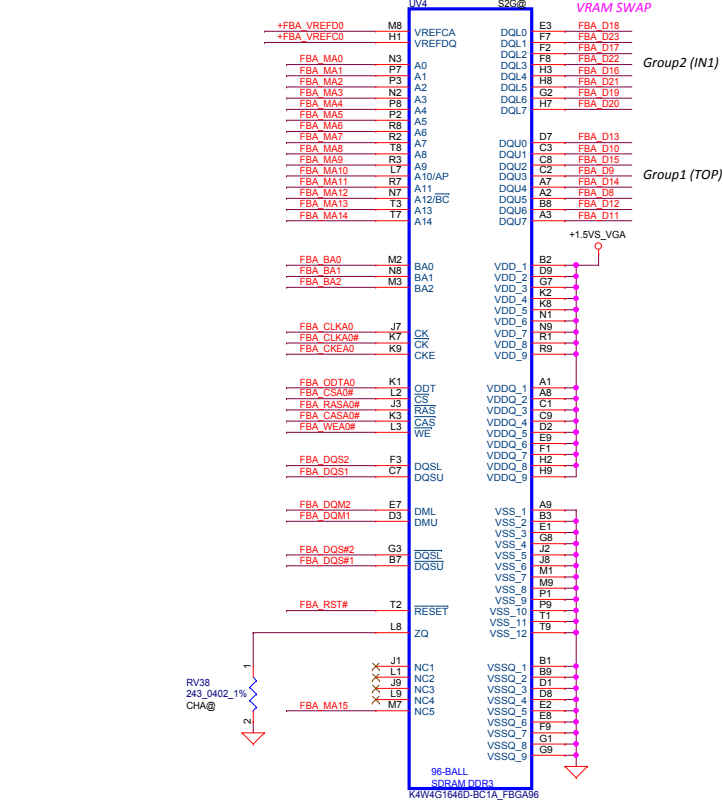



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Change all VRAM footprint to MT41K256M16HA107_FBGA_96P-A39P



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Memory Partition A - Upper 32 bits

Group 6 (BOT)

Group 7 (IN3)

Vram Swap

Group 4 (IN1)

Group 5 (TOP)

Legend:

- FBA_MA[15..0] <24,25>
- FBA_BA[2..0] <24,25>
- FBA_DQS[7..0] <24,25>
- FBA_DQM[7..0] <24,25>
- FBA_DQS[7..0] <24,25>
- FBA_DQ[0..63] <24,25>

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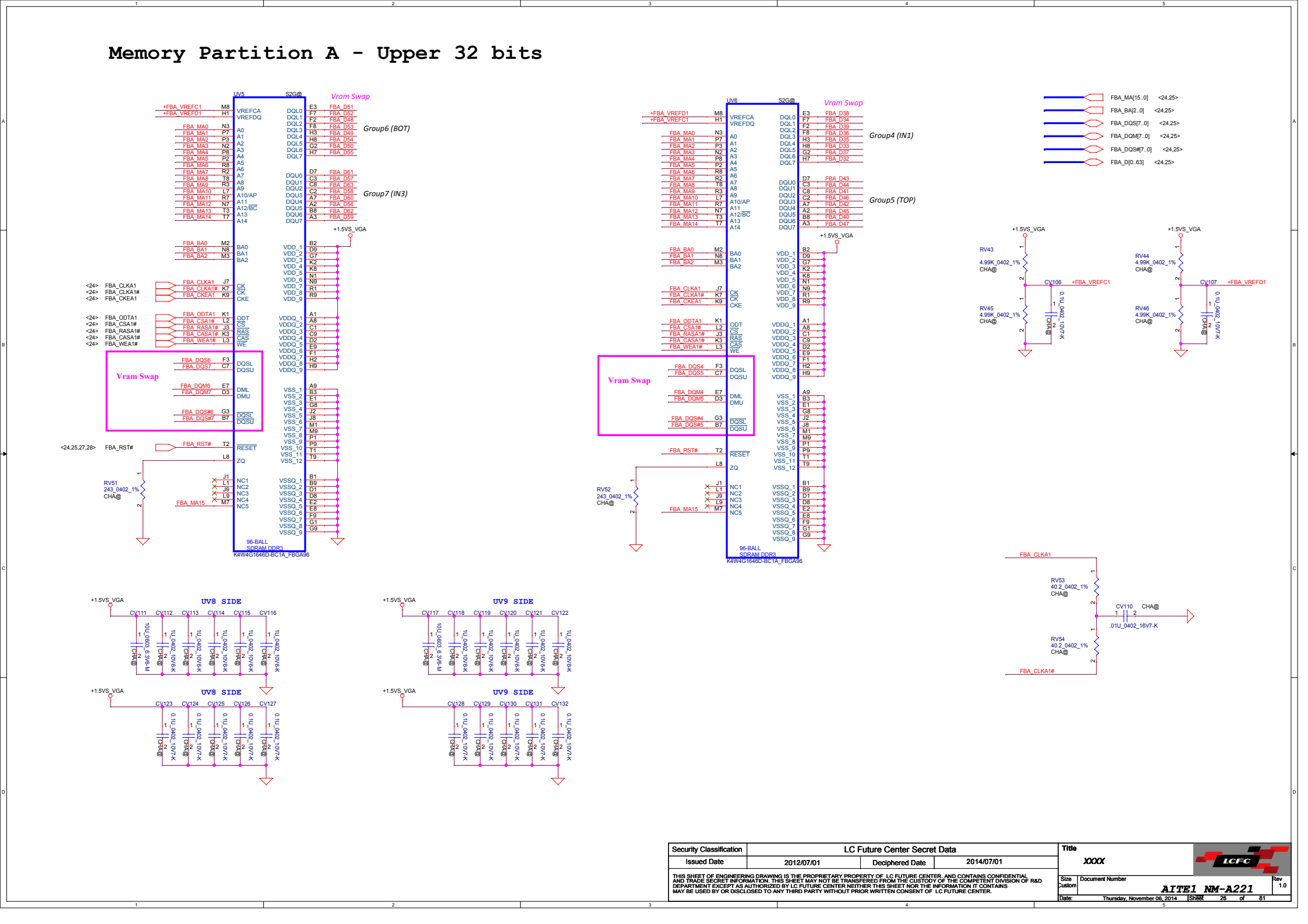
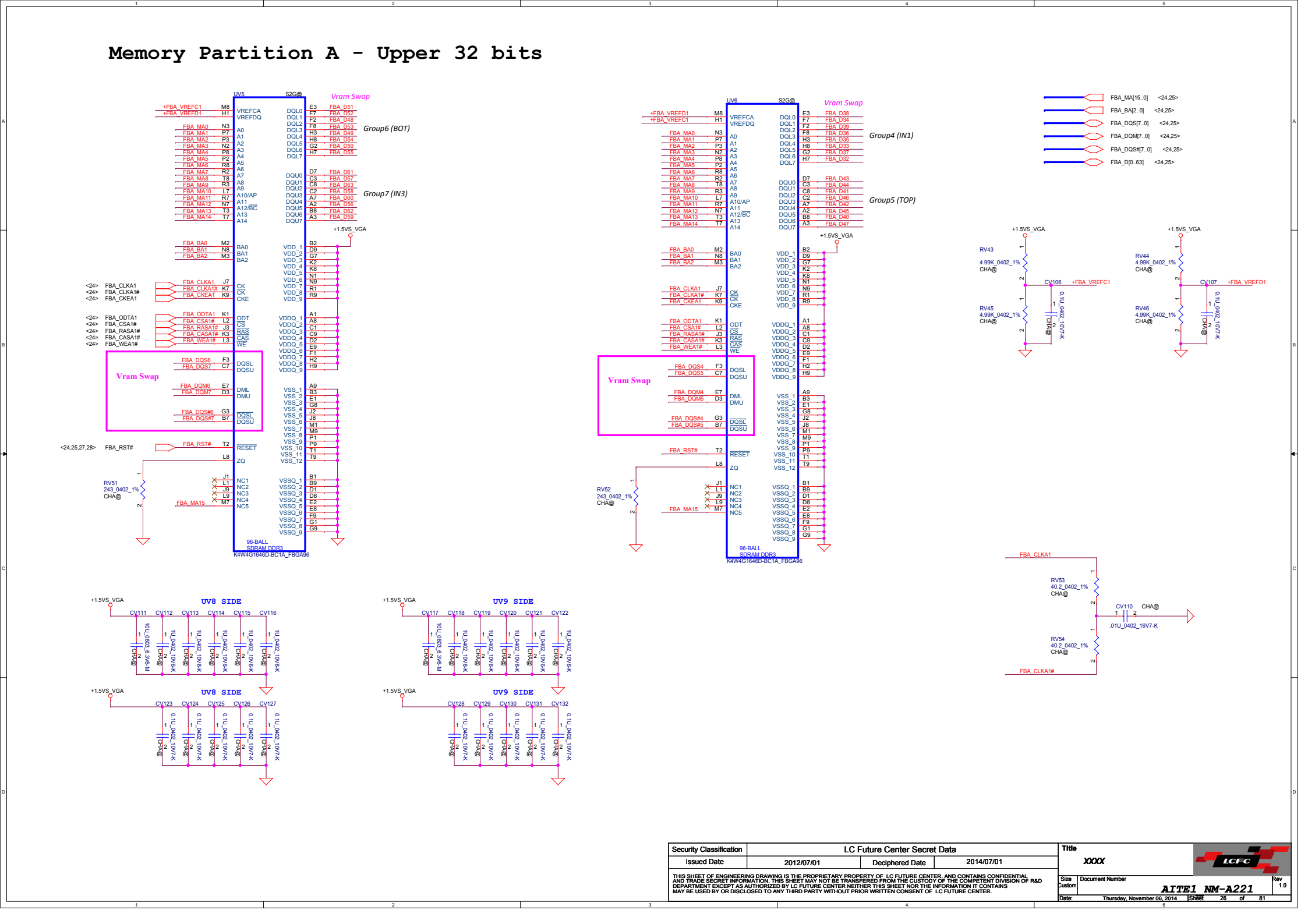
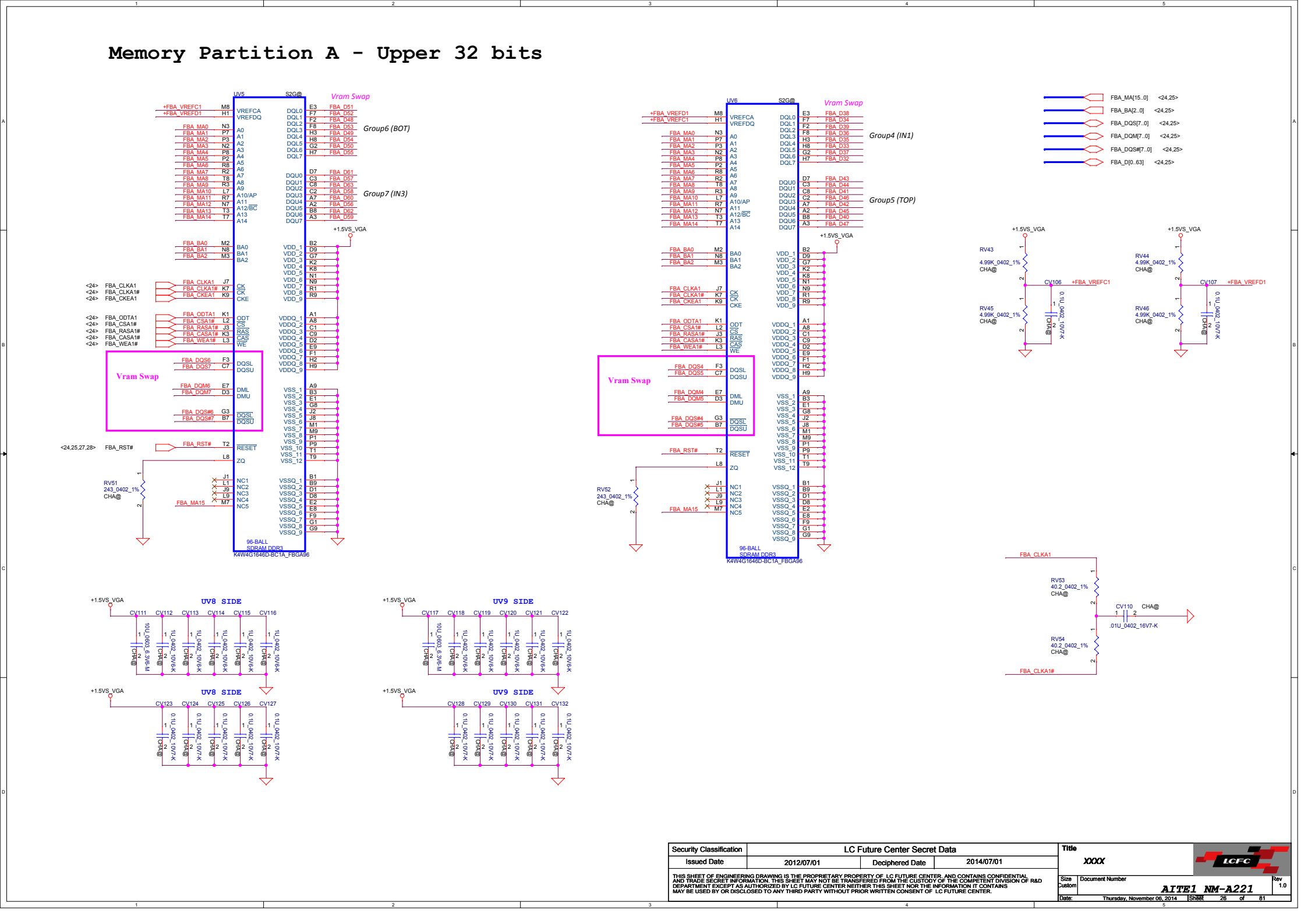
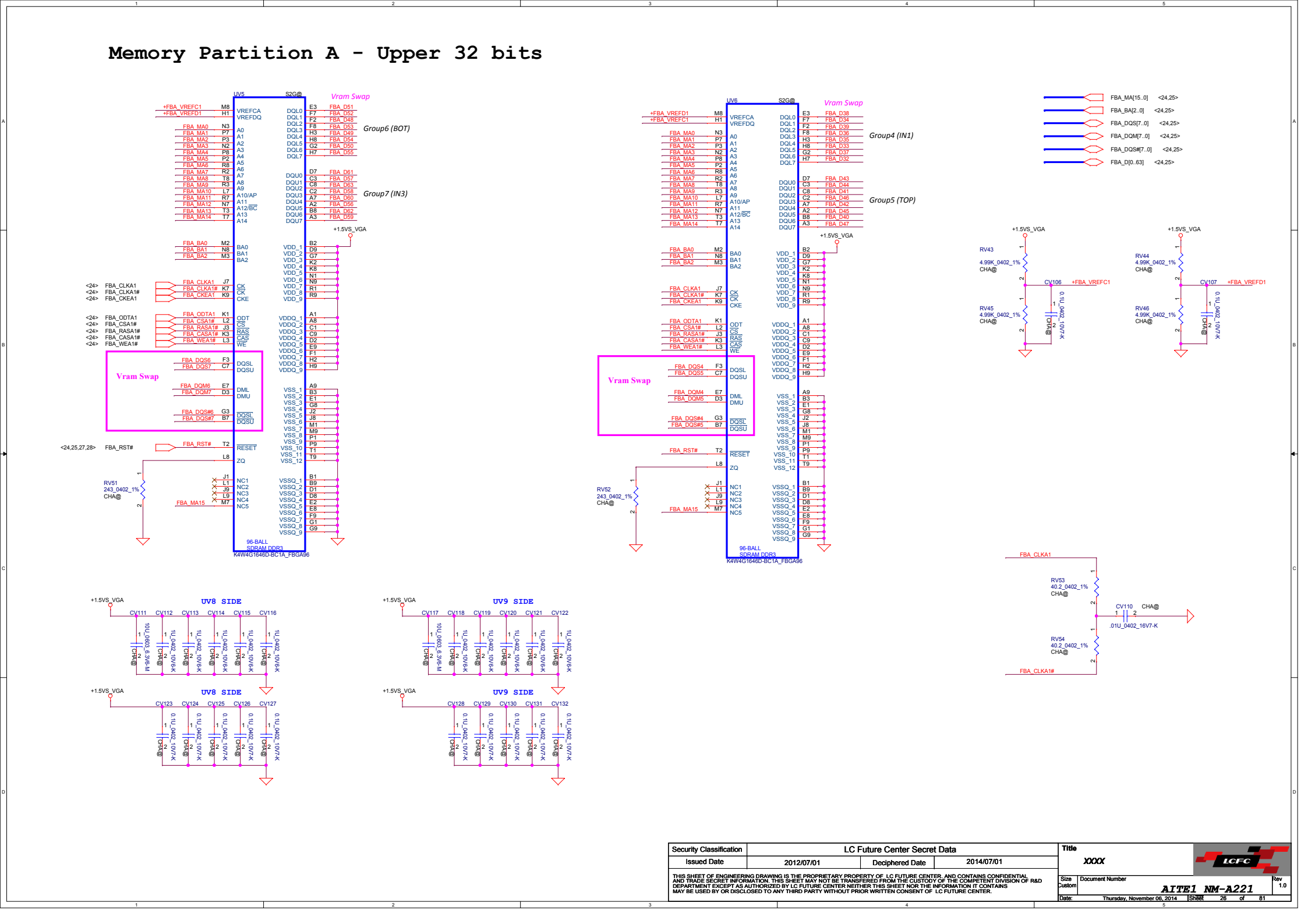
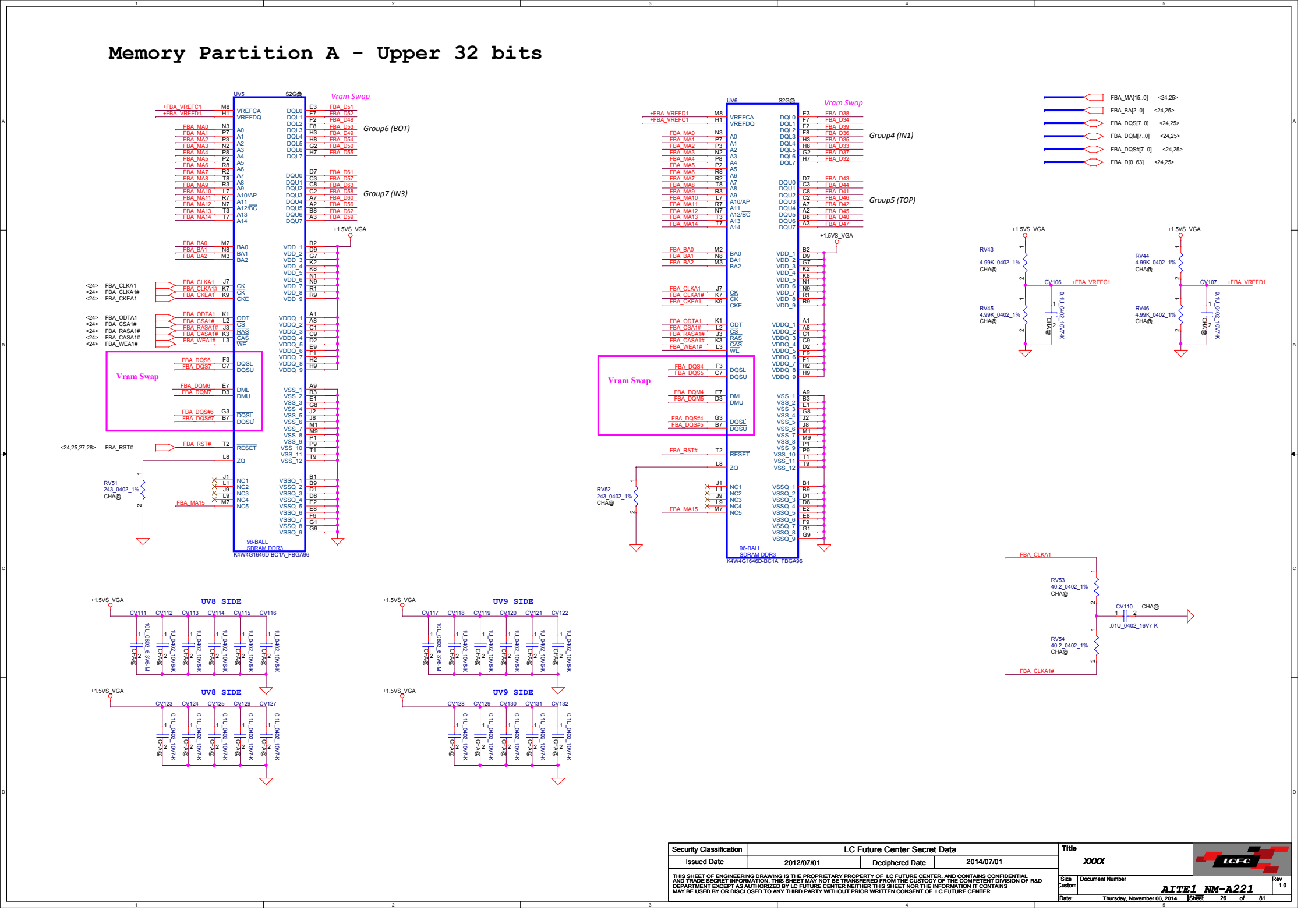
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Document Number AITE1 NM-A221

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Memory Partition A - Upper 32 bits

The diagram illustrates the electrical connections for Memory Partition A, specifically the upper 32 bits. It features two primary circuit boards, UV6 and UV9, which are populated with various memory modules and control logic.

UV6 Board Details:

- Vram Swap:** Includes components such as FBA MA0-M14, FBA BA0-BA2, FBA CLK1#, FBA CKE1#, FBA ODTA1, FBA CSA1#, FBA RAS1#, FBA WE1#, FBA DQS6-F7, FBA DOM6-D3, FBA DQS#6-B7, FBA RST#, and FBA MA15.
- Connectors:** J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88, J89, J90, J91, J92, J93, J94, J95, J96, J97, J98, J99, J100.
- Power and Grounding:** +1.5VS_VGA, VDD_1, VDD_2, VDD_3, VDD_4, VDD_5, VDD_6, VDD_7, VDD_8, VDD_9, VSS_1, VSS_2, VSS_3, VSS_4, VSS_5, VSS_6, VSS_7, VSS_8, VSS_9, VSS_10, VSS_11, VSS_12.

UV9 Board Details:

- Vram Swap:** Similar to UV6, but with specific component variations.
- Connectors:** J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88, J89, J90, J91, J92, J93, J94, J95, J96, J97, J98, J99, J100.
- Power and Grounding:** +1.5VS_VGA, VDD_1, VDD_2, VDD_3, VDD_4, VDD_5, VDD_6, VDD_7, VDD_8, VDD_9, VSS_1, VSS_2, VSS_3, VSS_4, VSS_5, VSS_6, VSS_7, VSS_8, VSS_9, VSS_10, VSS_11, VSS_12.

Signal Traces and Components:

- FBA_MA[15..0] <24,25>**, **FBA_BA[2..0] <24,25>**, **FBA_DQS[7..0] <24,25>**, **FBA_DQM[7..0] <24,25>**, **FBA_DQS#[7..0] <24,25>**, **FBA_D[0..63] <24,25>**.
- FBA_CLKA1**, **FBA_CLKA1#**.
- RV33**, **RV34**, **CV110**, **CV111**, **CV112**, **CV113**, **CV114**, **CV115**, **CV116**, **CV117**, **CV118**, **CV119**, **CV120**, **CV121**, **CV122**, **CV123**, **CV124**, **CV125**, **CV126**, **CV127**, **CV128**, **CV129**, **CV130**, **CV131**, **CV132**.

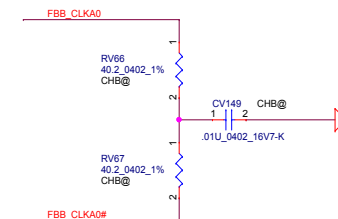
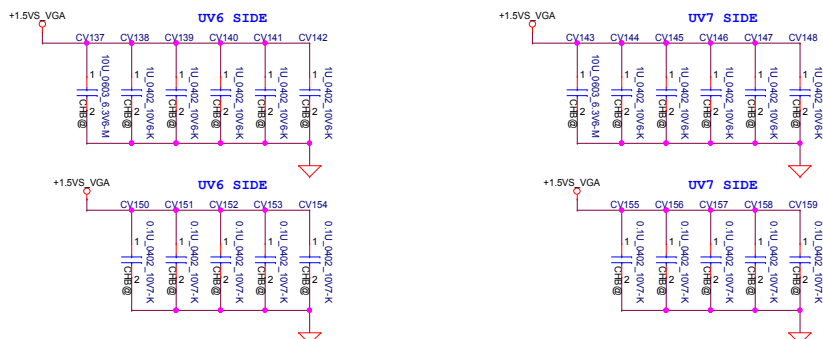
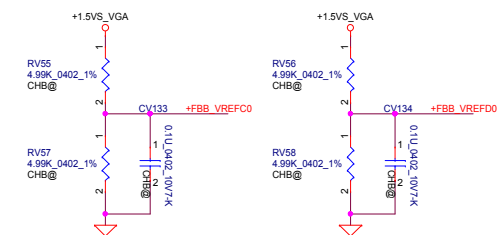
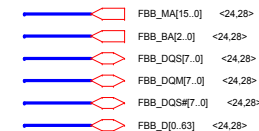
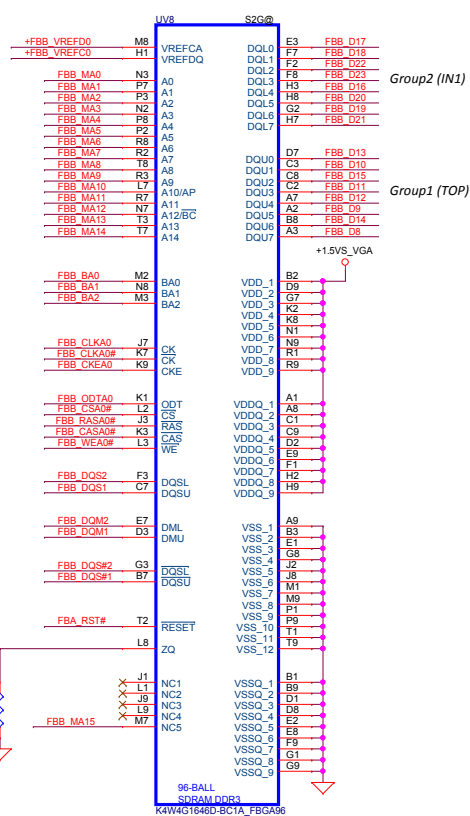
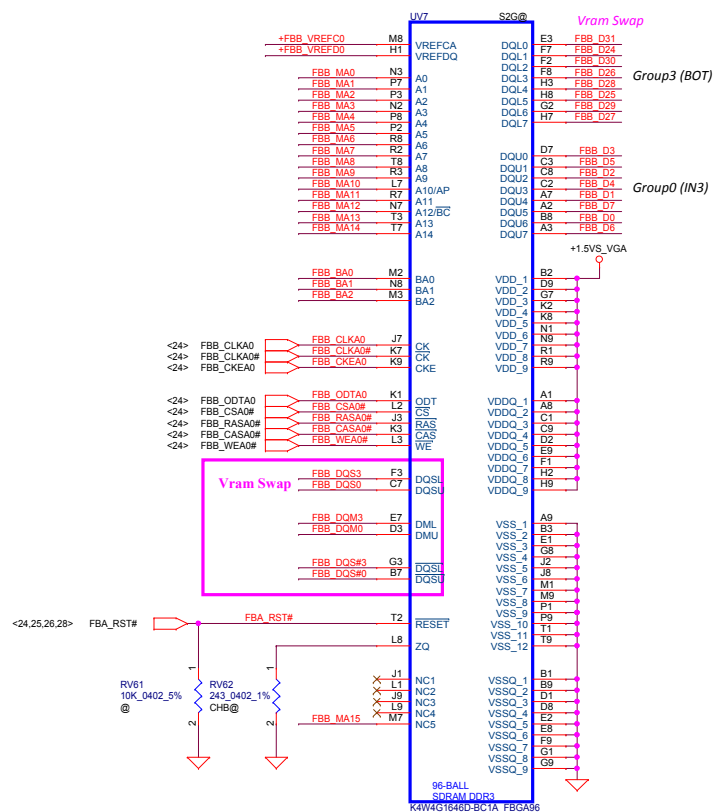
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Issued Date	2012/07/01	Deciphered Date	2014/07/01

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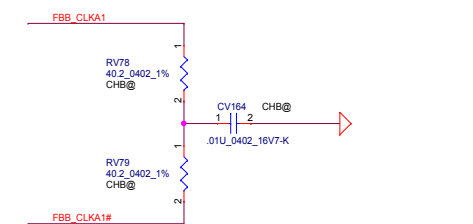
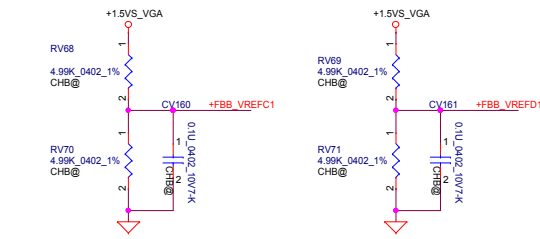
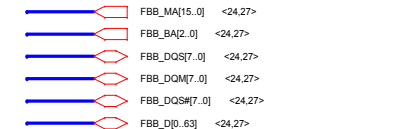
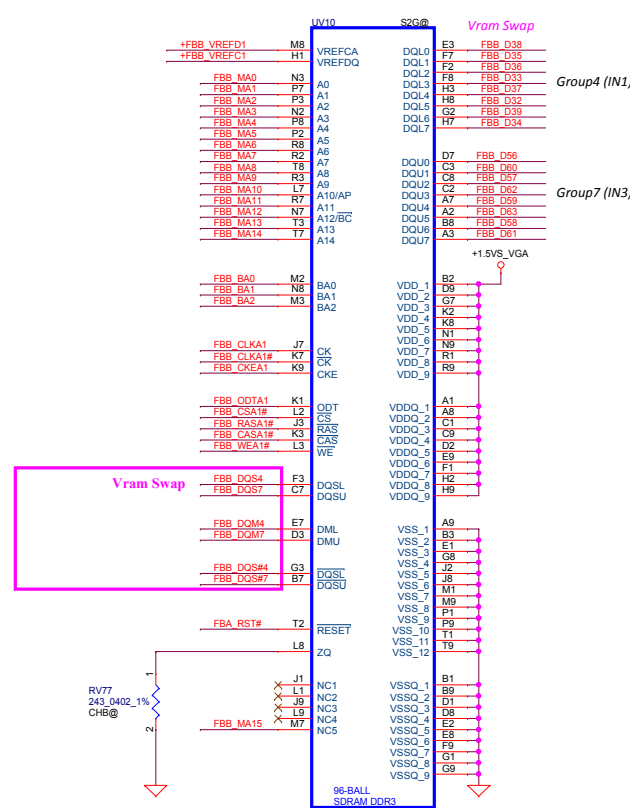
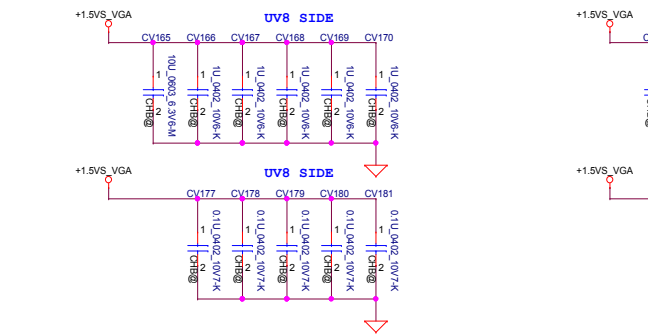
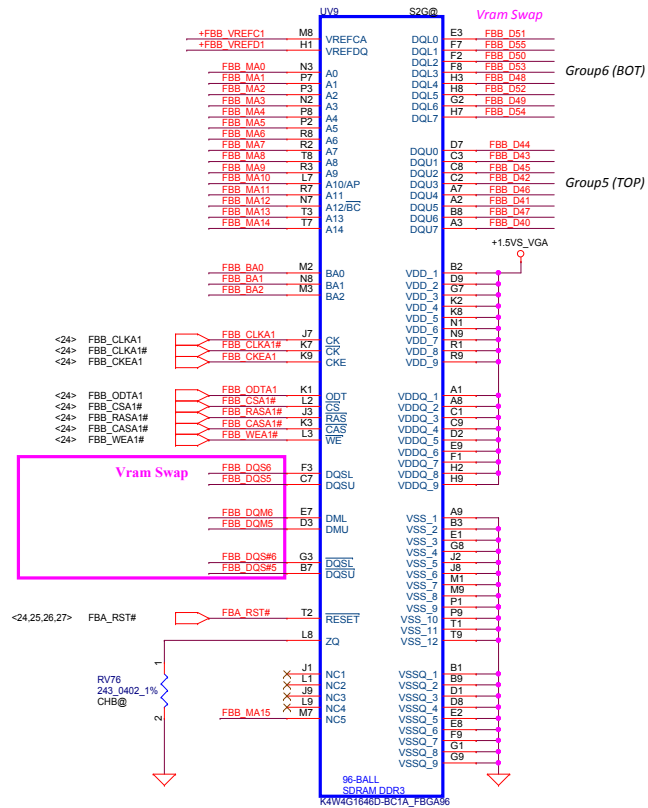
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 Document Number: AITE1 NM-A221
 Date: Thursday, November 06, 2014
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Memory Partition A - Lower 32 bits

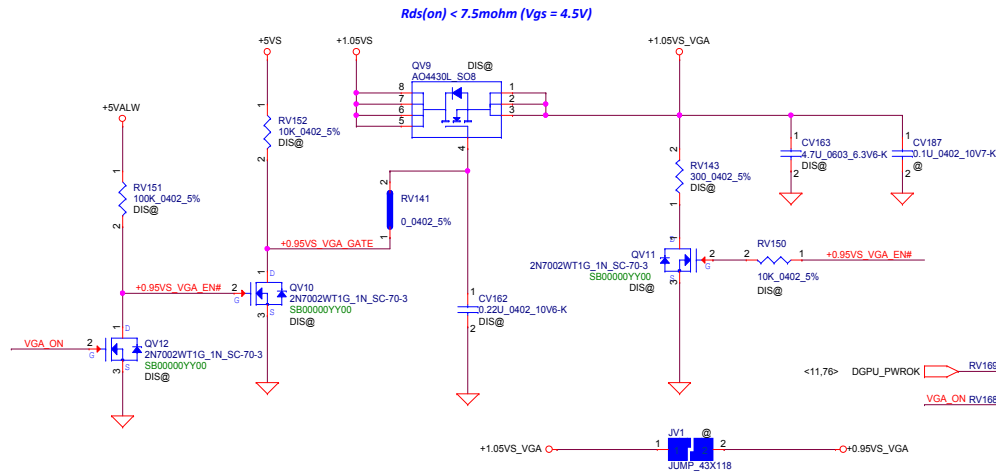


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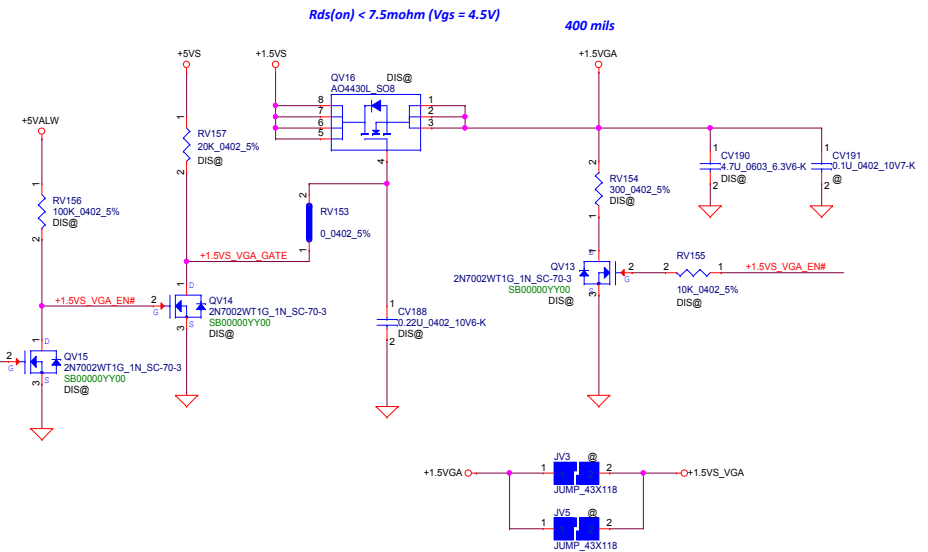
Memory Partition A - Upper 32 bits



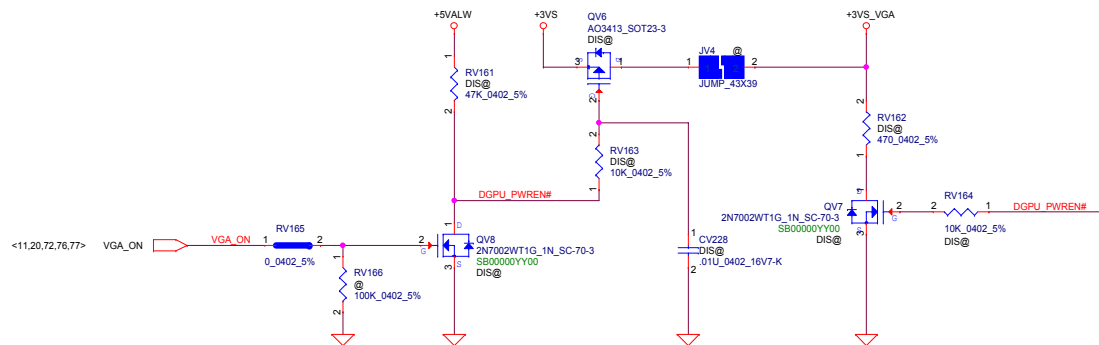
+1.05VS to +0.95VS_VGA



+1.5VS to +1.5VS_VGA




+3VS to +3VS_VGA




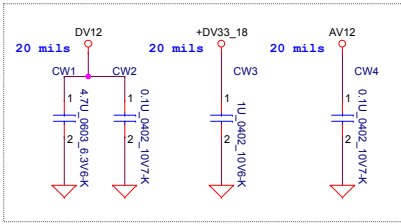
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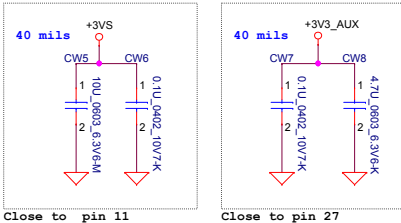
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Date:				Thursday, November 06, 2014 Sheet 31 of 81			

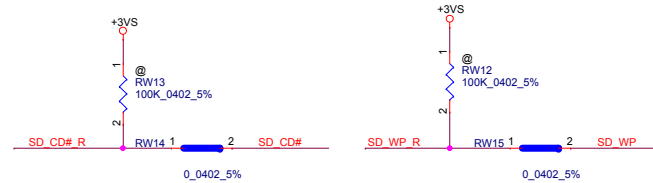
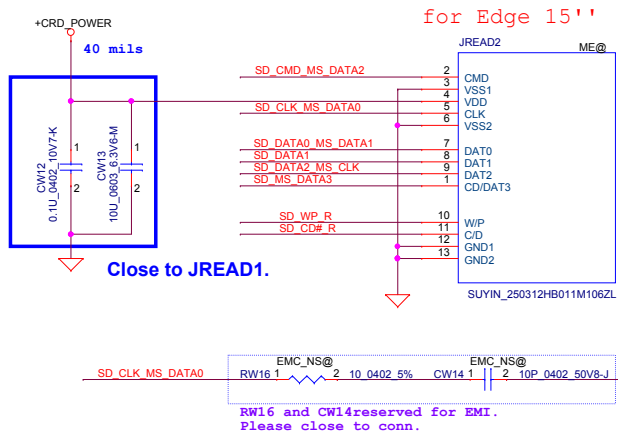
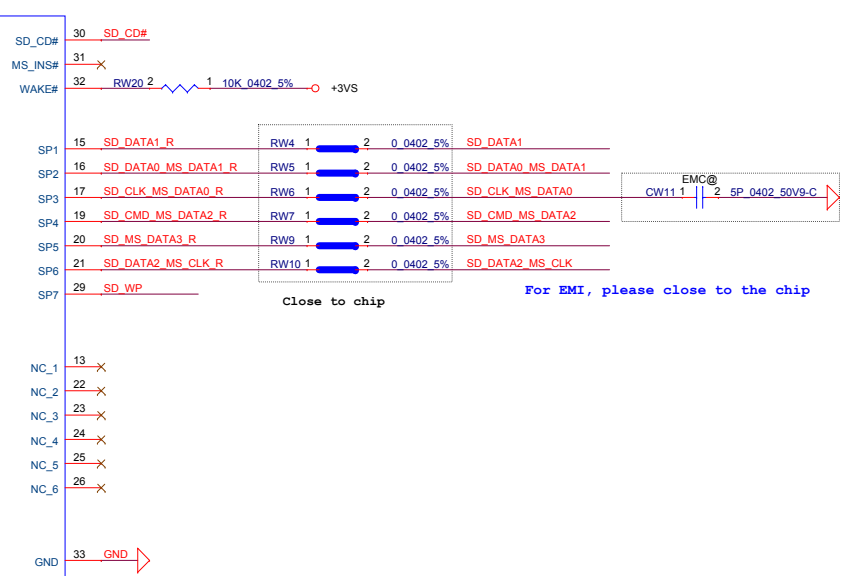
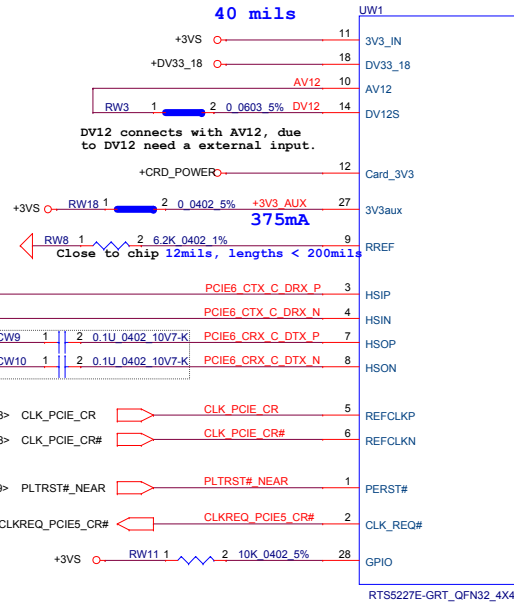


All of cap. close to chip




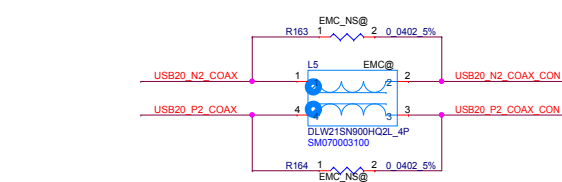
Close to pin 11

Close to pin 27



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(Move to sub board)

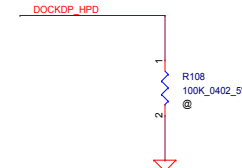
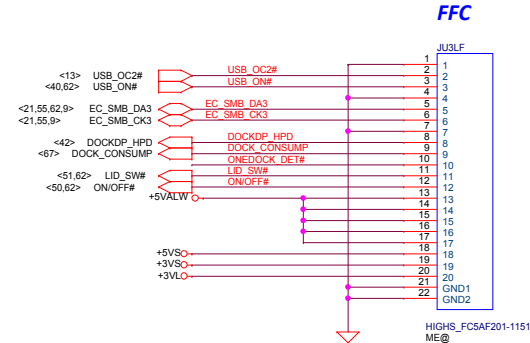
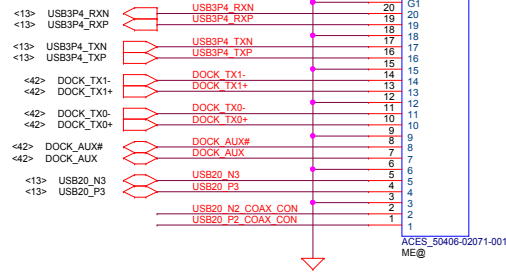
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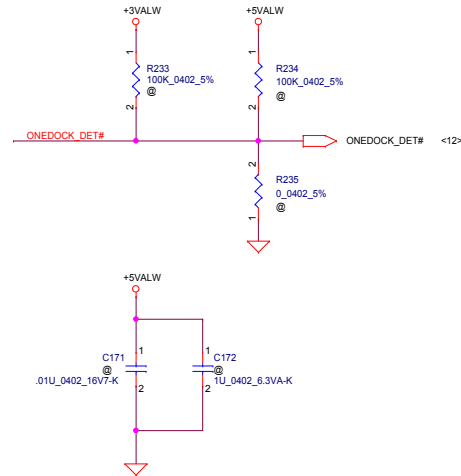
DOCKING

DOCKING

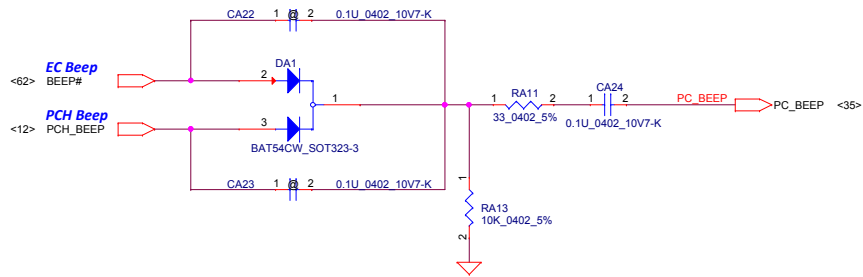
SUB/B



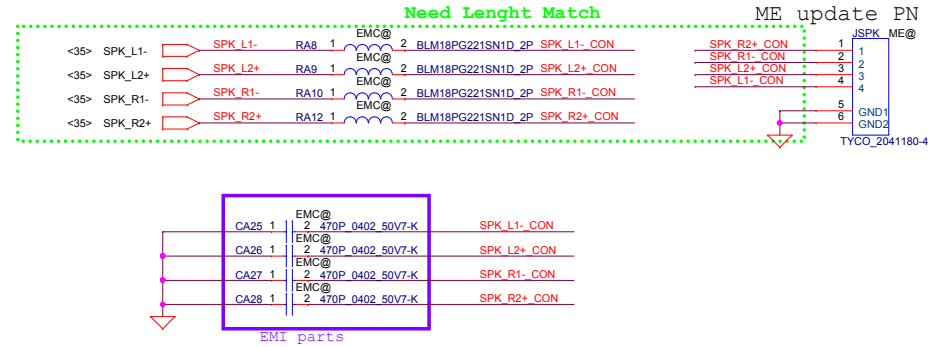
1. AC Capacitor place on Sub/B
2. Need to check with MUX IC vendor whether still need AC cap between MUX IC and device.



PC BEEP

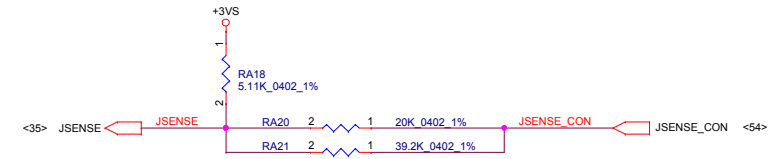
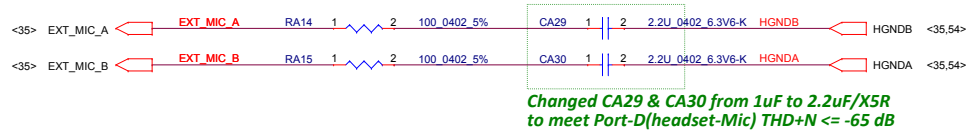


Speaker OUT

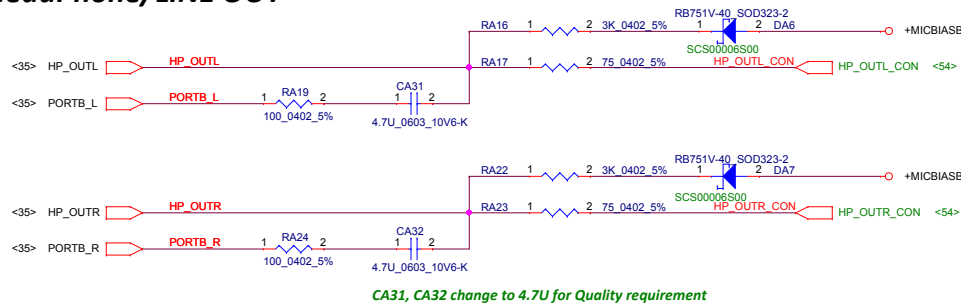


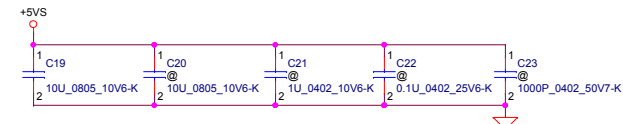
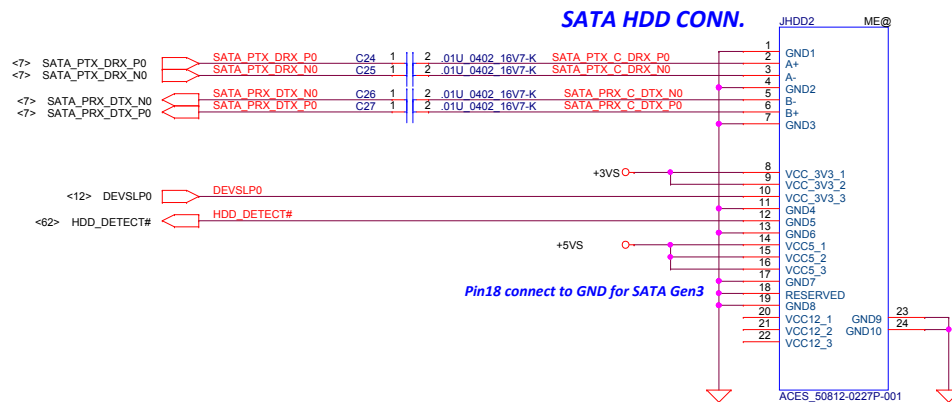
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A

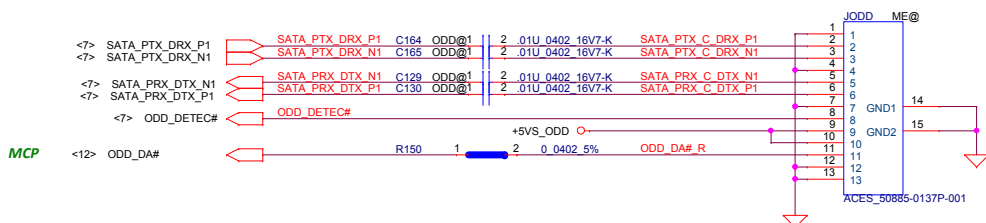


HeadPhone/LINE OUT

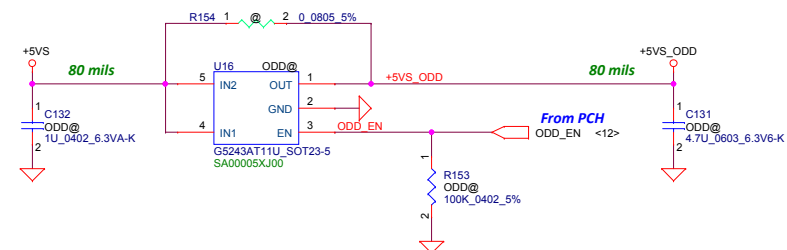




SATA ODD CONN

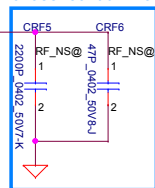



+5VS TO +5VS_ODD



+5VS_ODD

For RF solution.
Close to JODD connector.



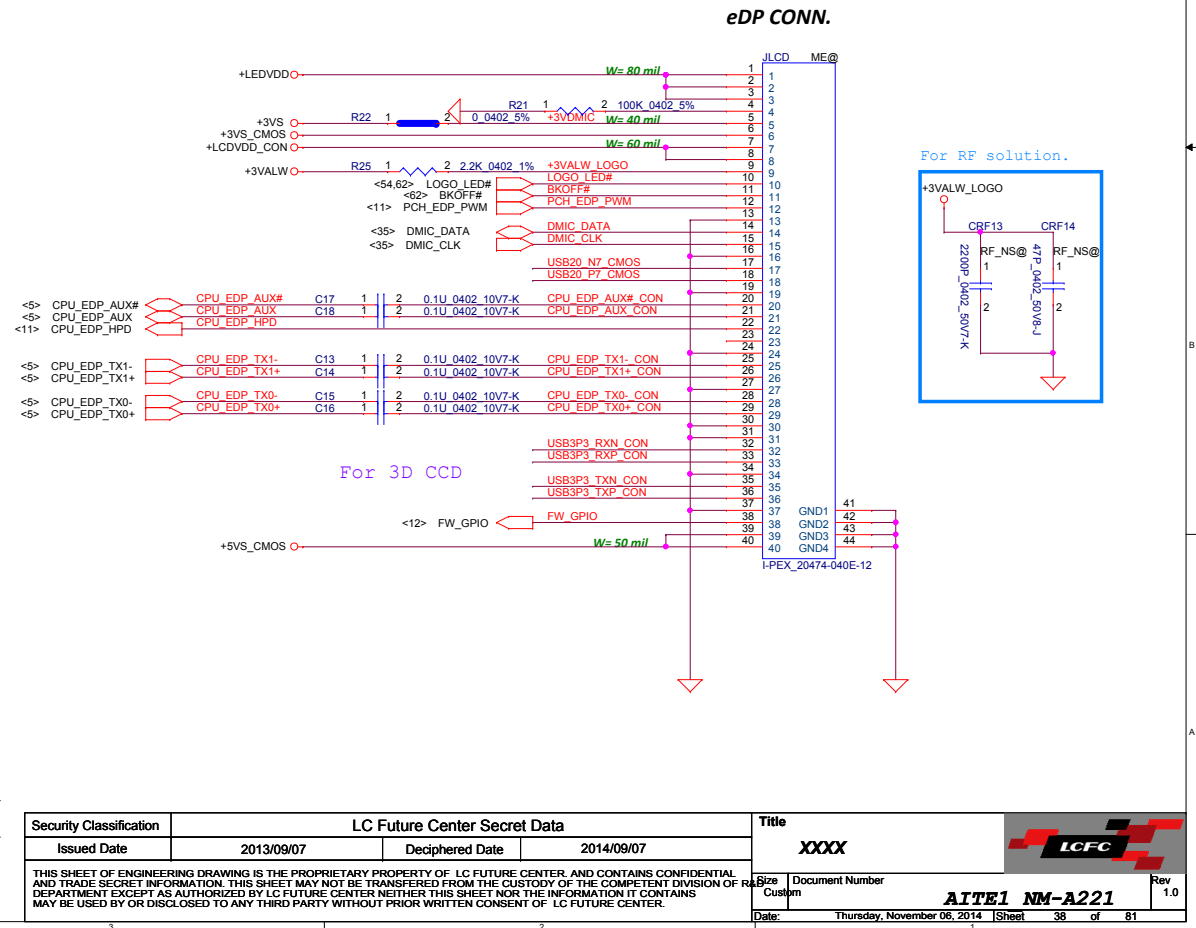
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[illegible]


For 2D CCD

For 3D CCD

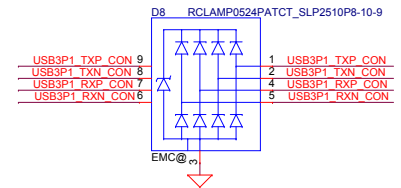
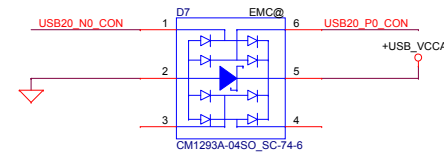
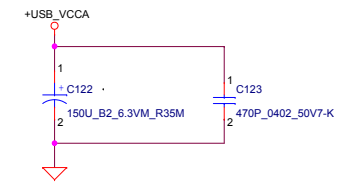
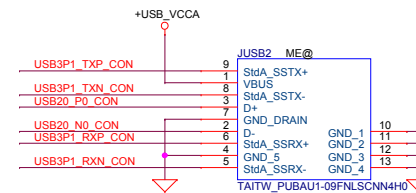
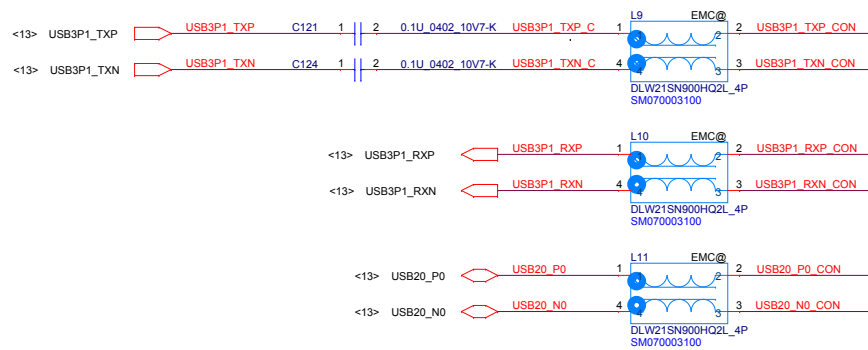
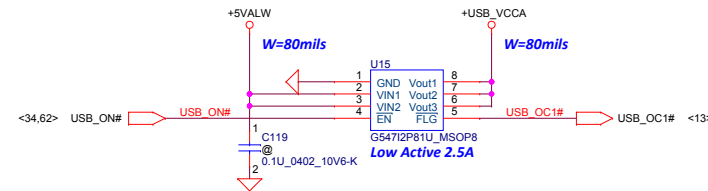
For RF solution.

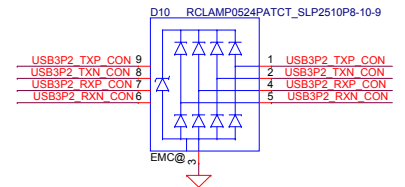
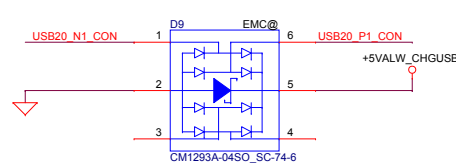
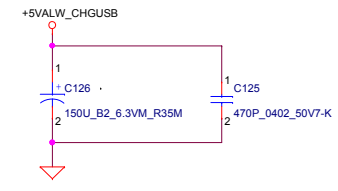
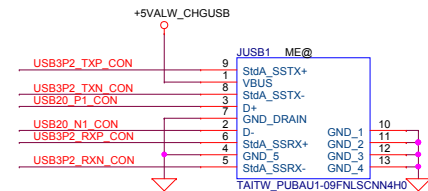
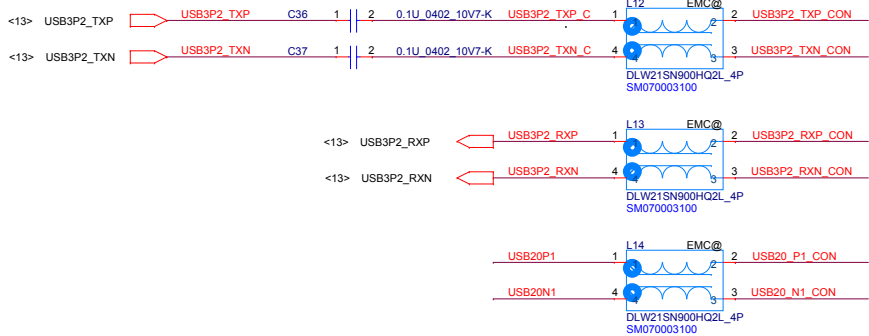
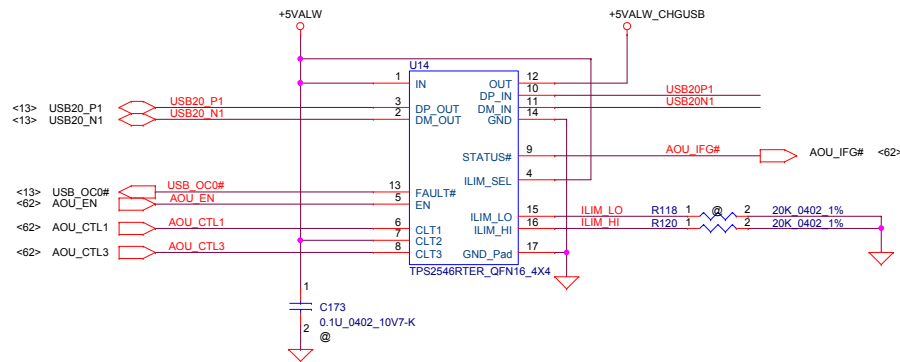


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POWER SWITCH





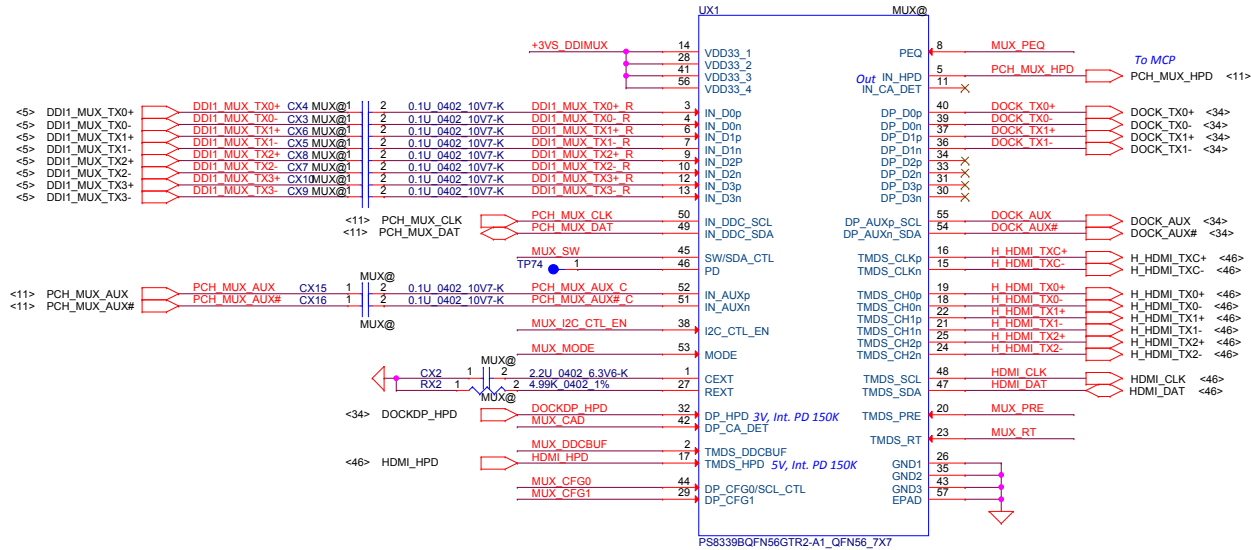
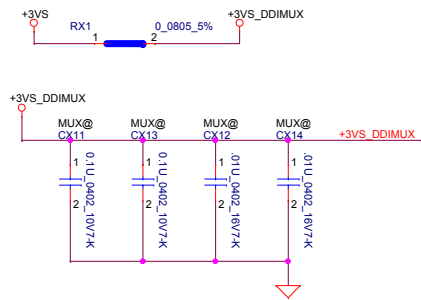
TI TPS2546

CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

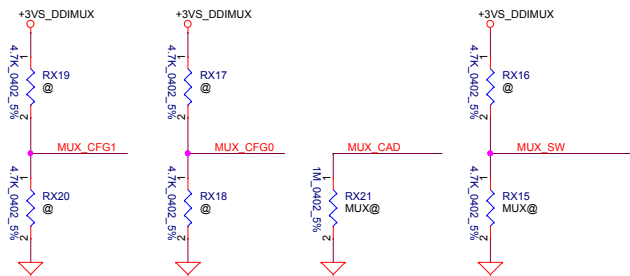
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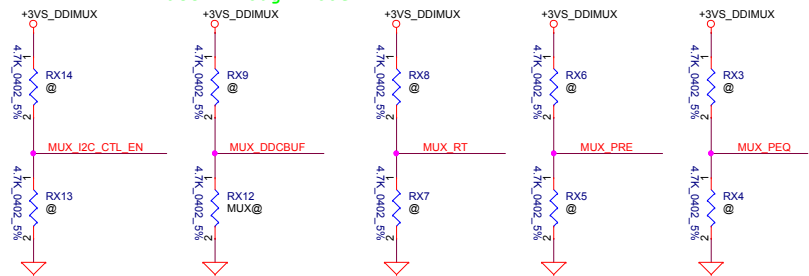
Rev 1.0




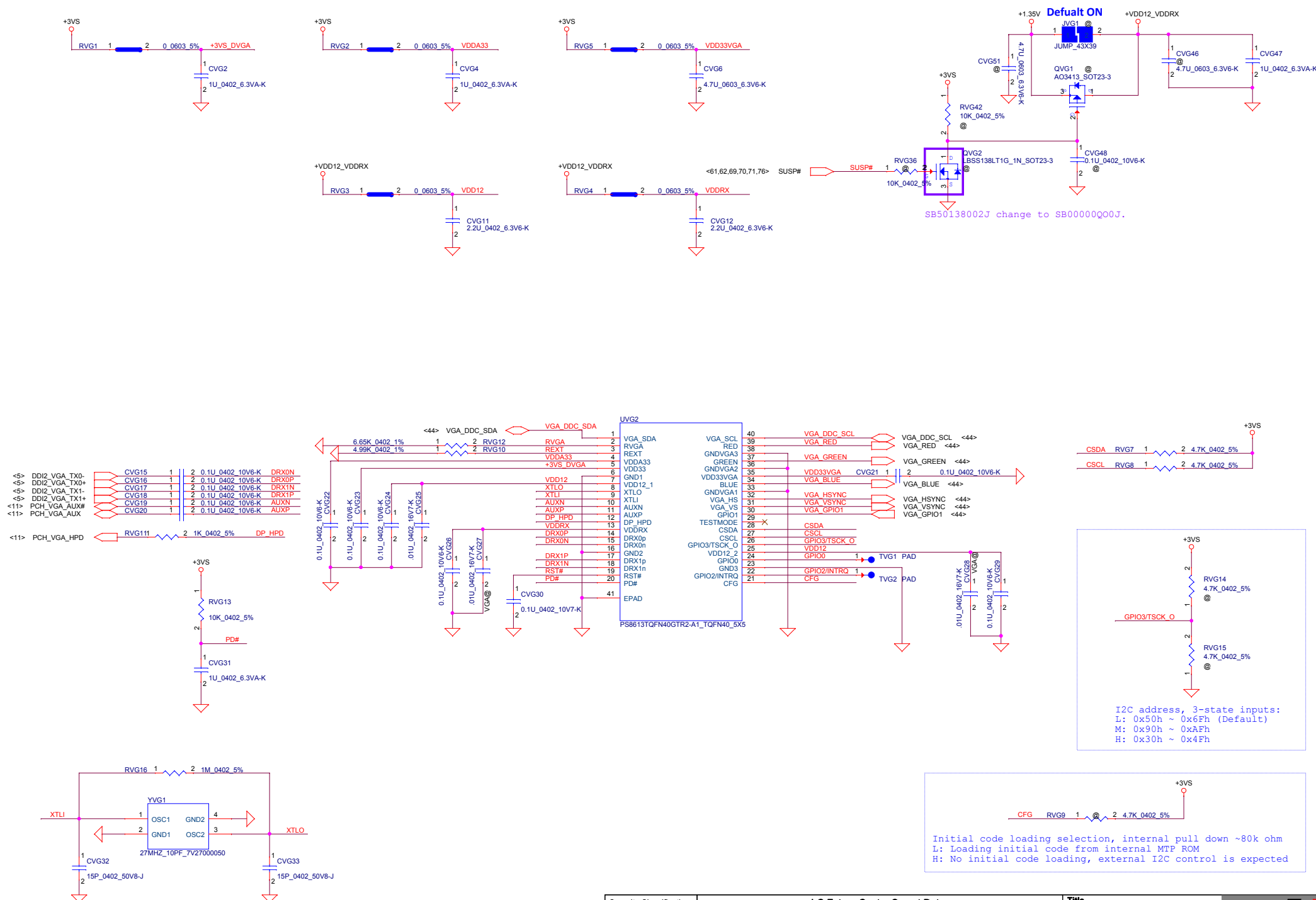
Auto Mode DP Higher Priority



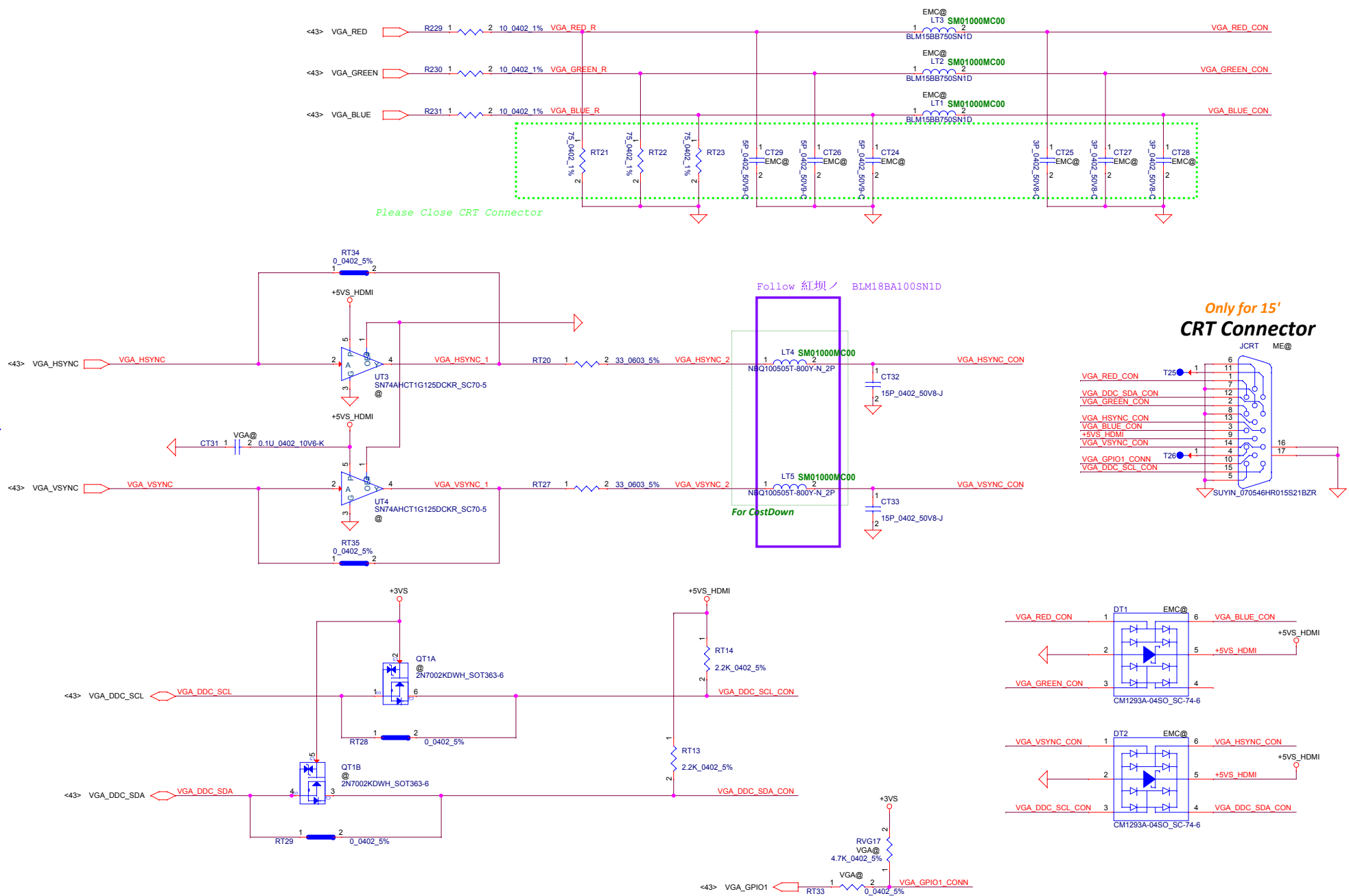
Pass Through Mode




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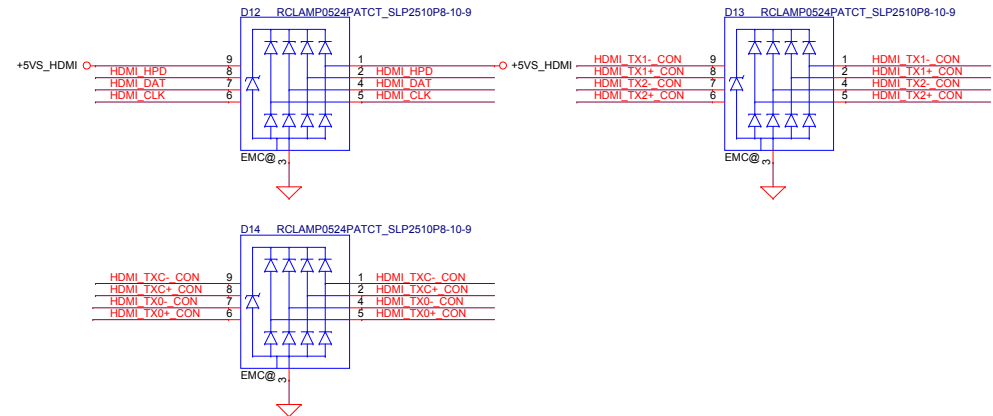
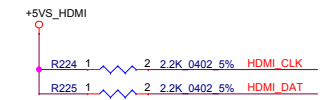
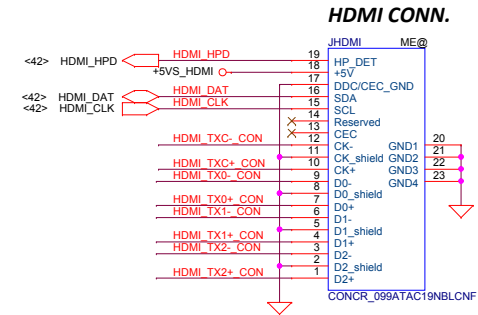
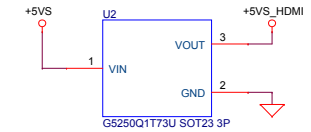
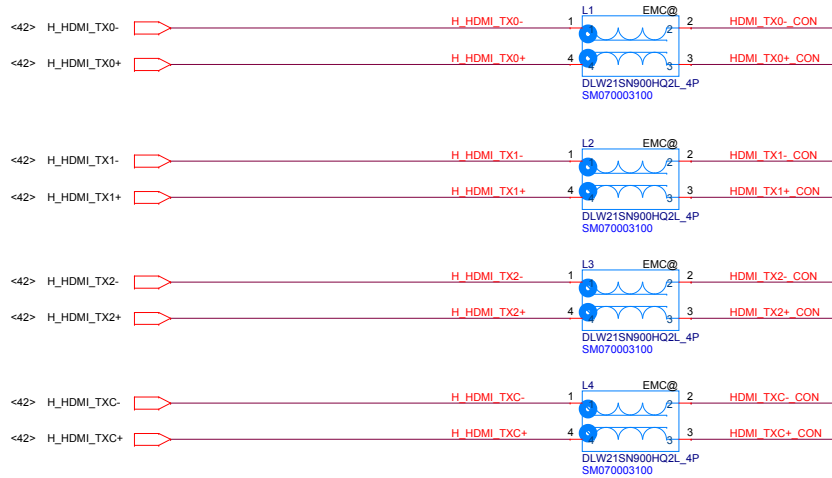


Traslater



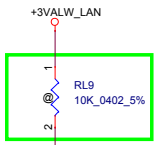
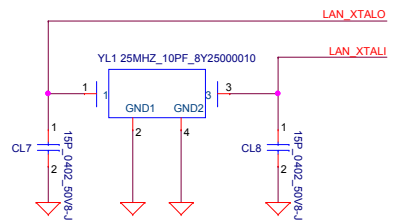
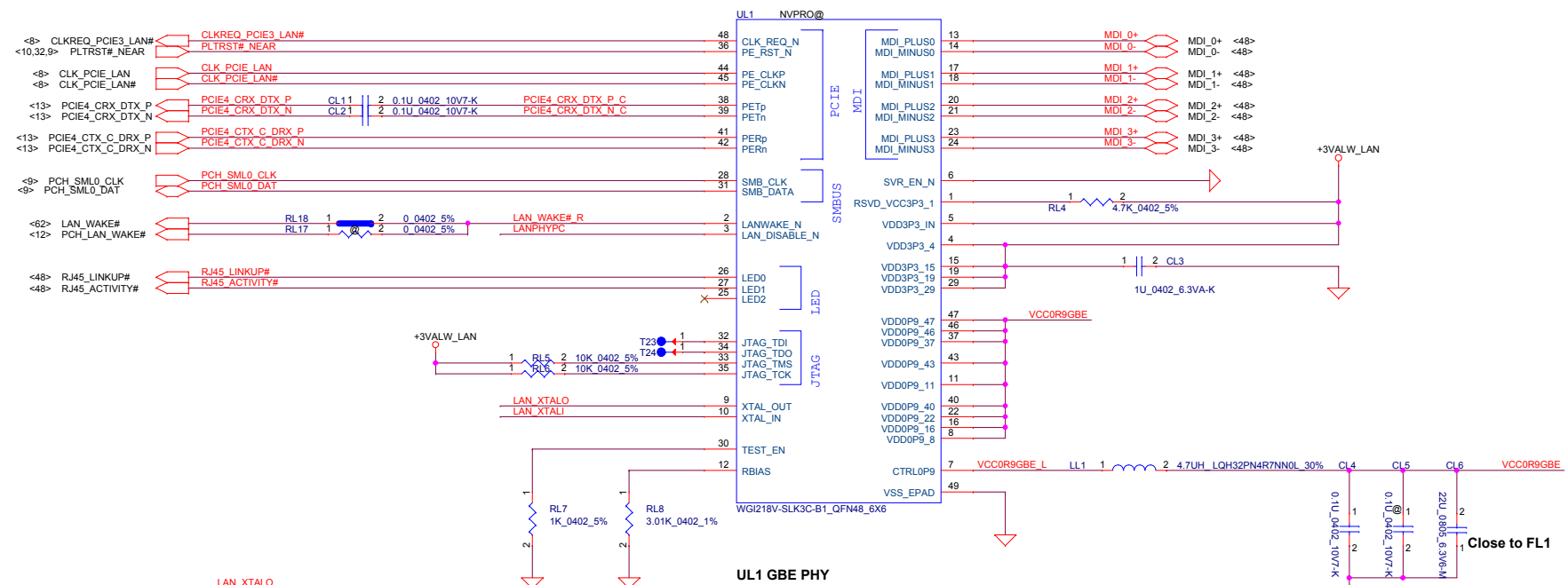
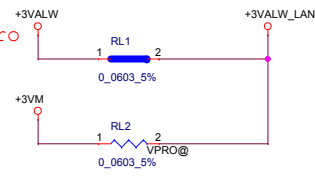
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For Non-Vpro

For Vpro



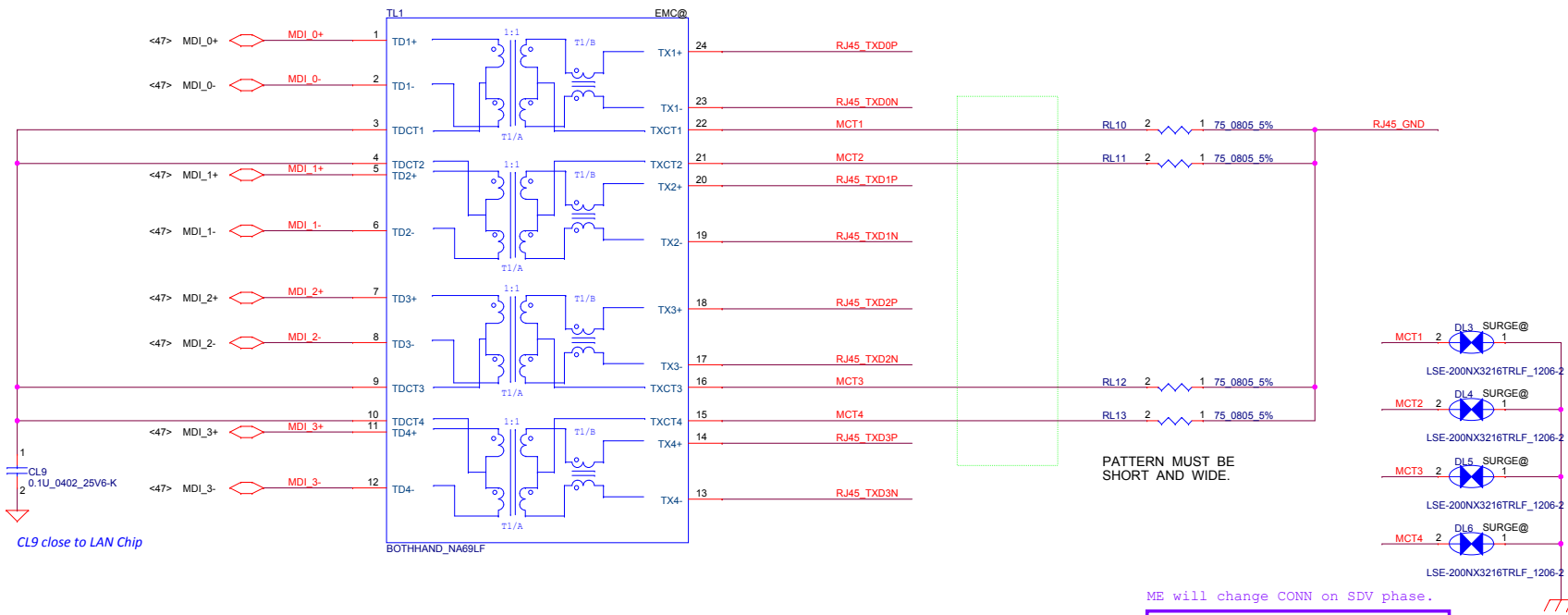
<12> LANPHYC

When use Native function, intel recommend pull high 10K ohm
This part is un-mount in Sting.

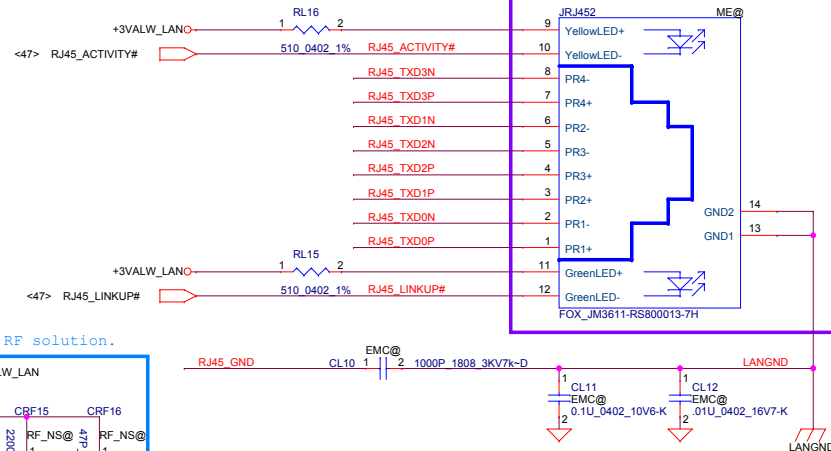
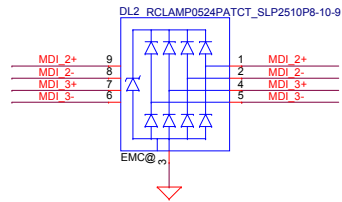
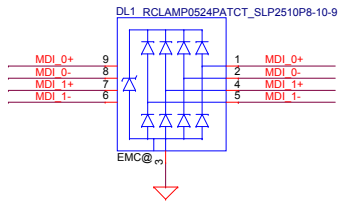
UL1 GBE PHY

vPro Model	Non-vPro Model
I218LM	I218V

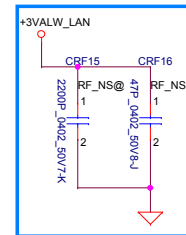
ST-1_SWG_SDV-SWG_EC062
Add vPro/Non-vPro table.



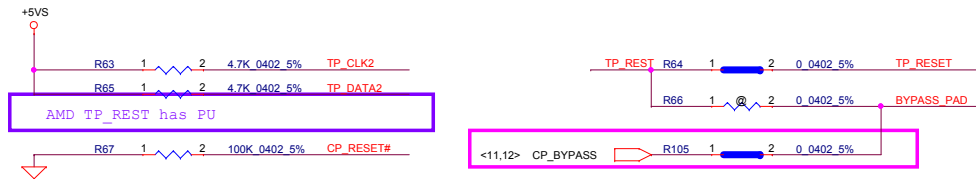
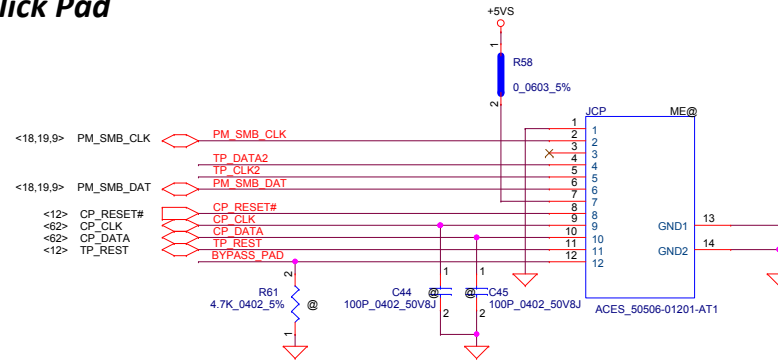
ME will change CONN on SDV phase.



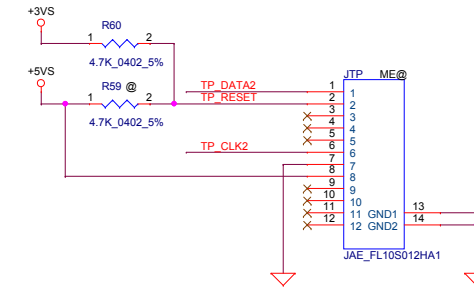
For RF solution.



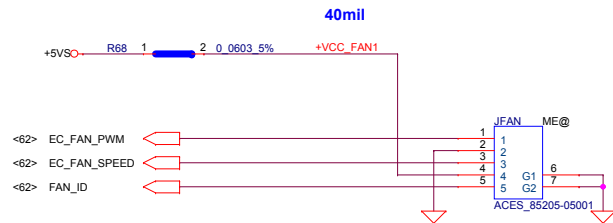
Click Pad



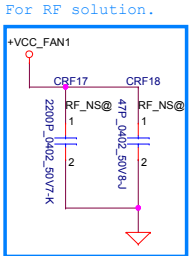
Track point



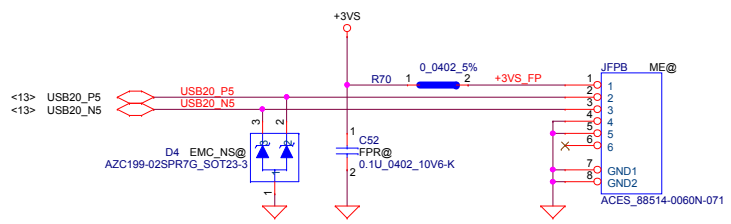
FAN CONN.



惠瑞鐵AMD鐵THERMAL紙板PIN define



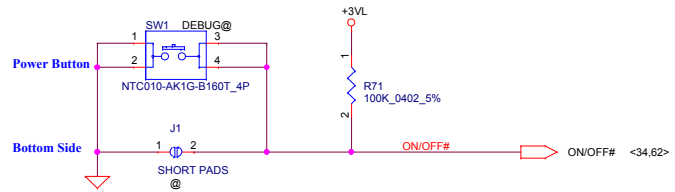
FingerPrint CONN.



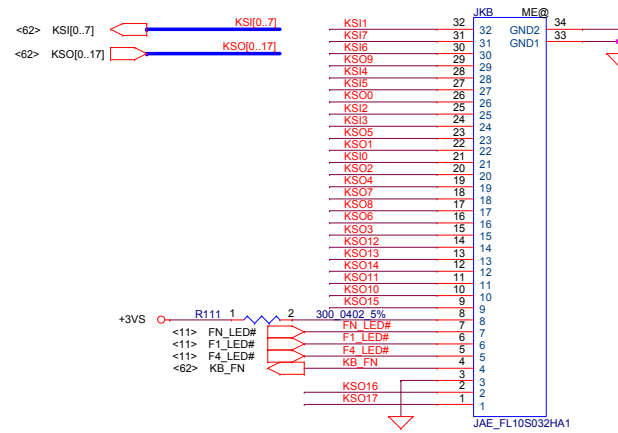
PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

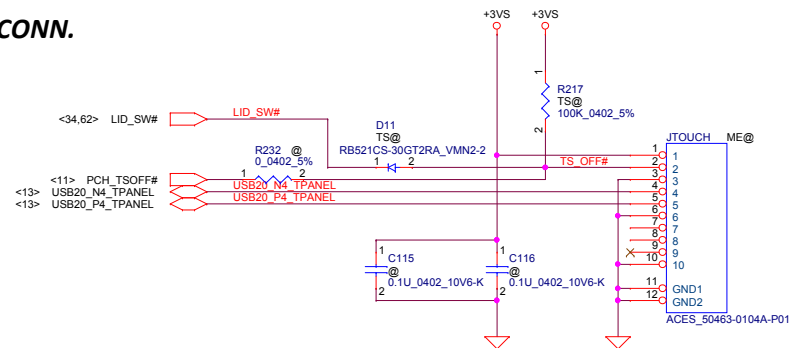
ON/OFF Switch --> 簿 Sub/B



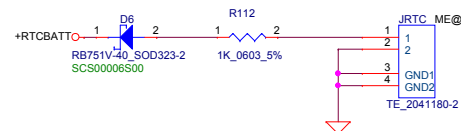
Lid Switch --> 簿 Sub/B


KB CONN

TOUCH PANEL CONN.

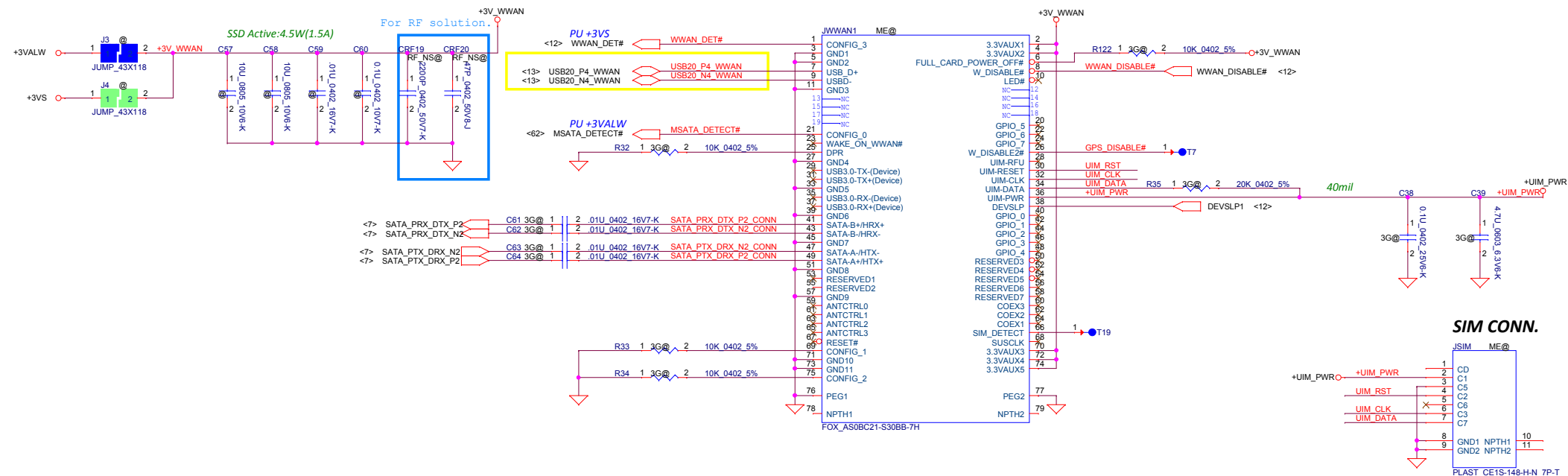


RTC CONN.

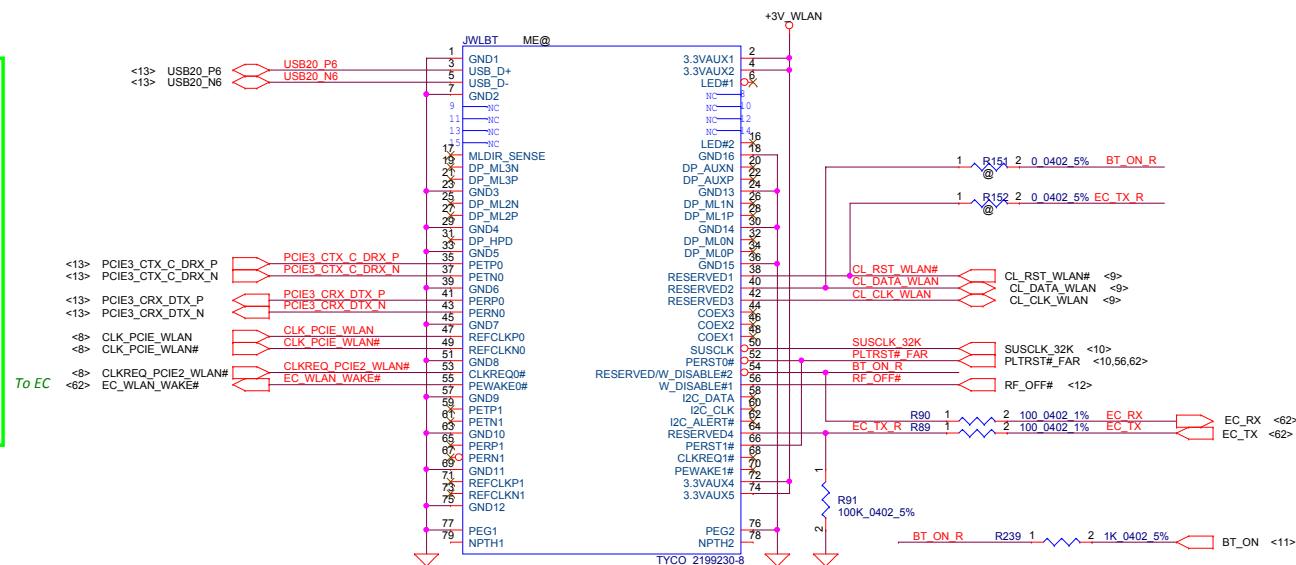
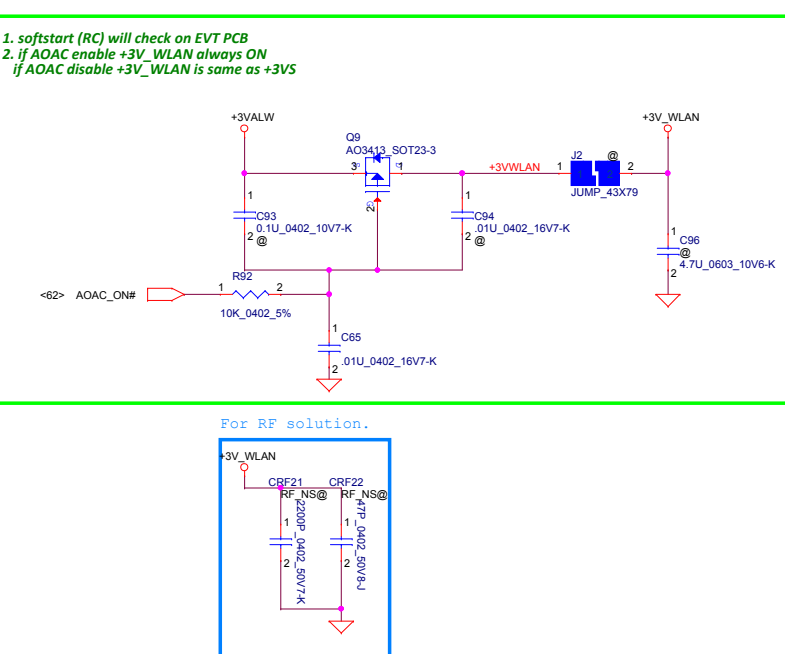



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				Date:	Thursday, November 06, 2014	Sheet	51 of 81

TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR




TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR

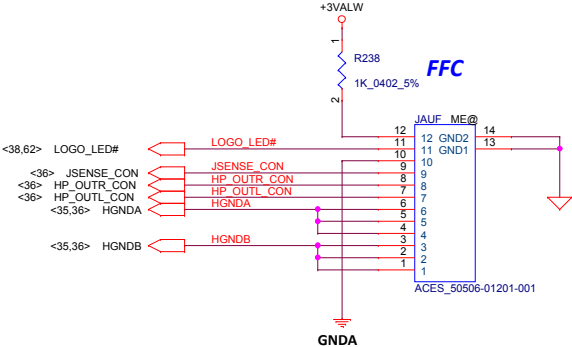


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Date: Thursday, November 06, 2014 15:52 of 11					Revision 1

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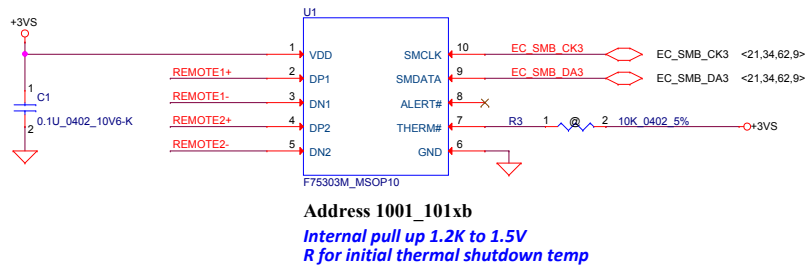
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For Edge 15" Audio board CONNECTOR

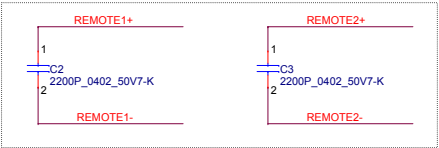


Thermal Sensor

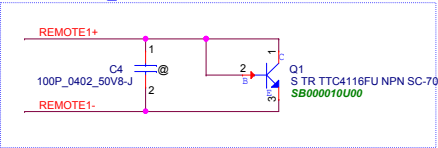
Thermal Sensor
placed near by VRAM



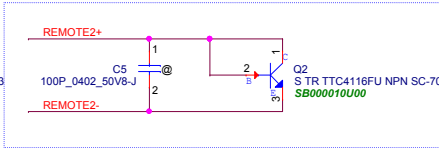
Close to U1



Close to +VCC_CORE



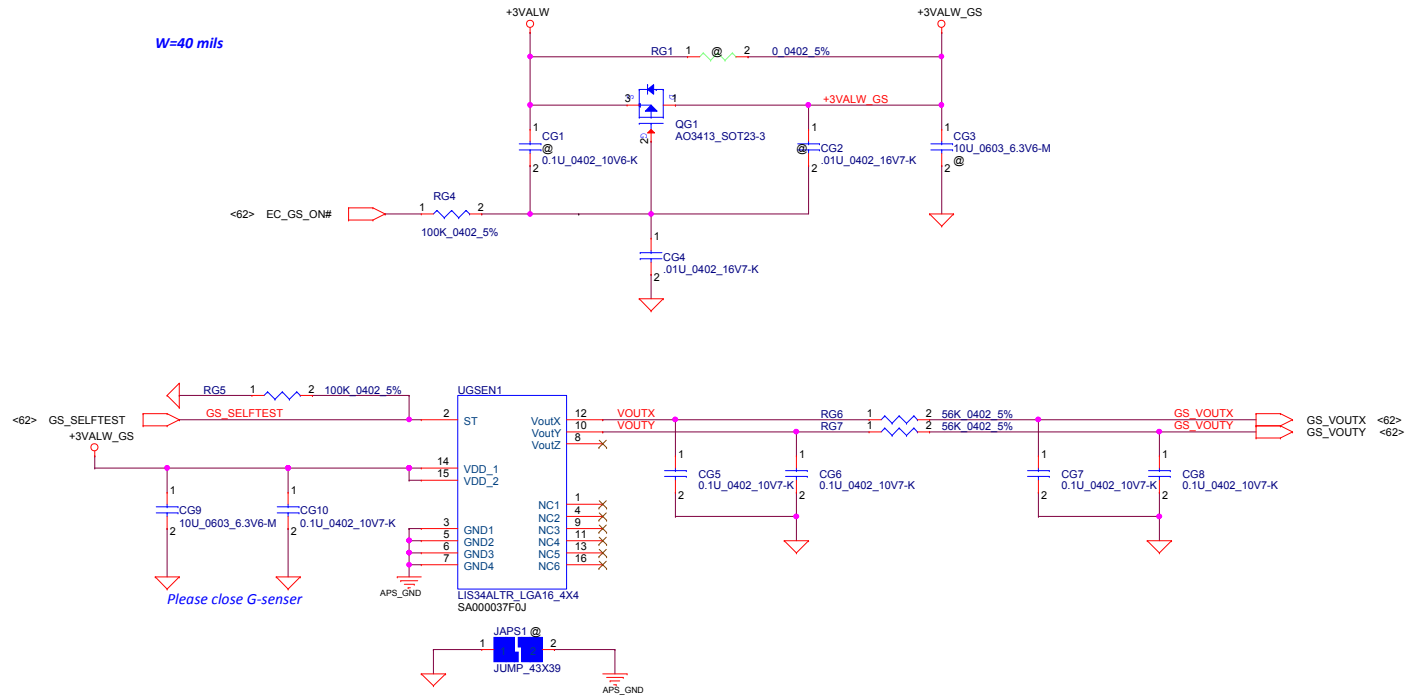
Close JDIMM1&JDIMM2



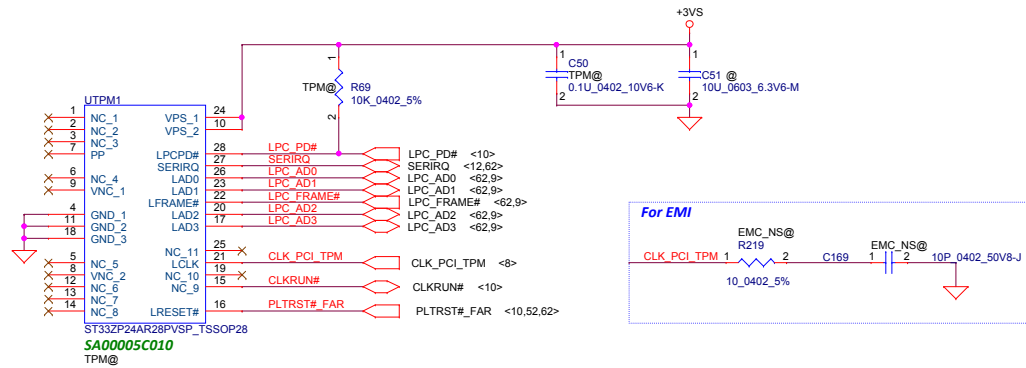
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"


APS G-Sensor

W=40 mils




TPM IC




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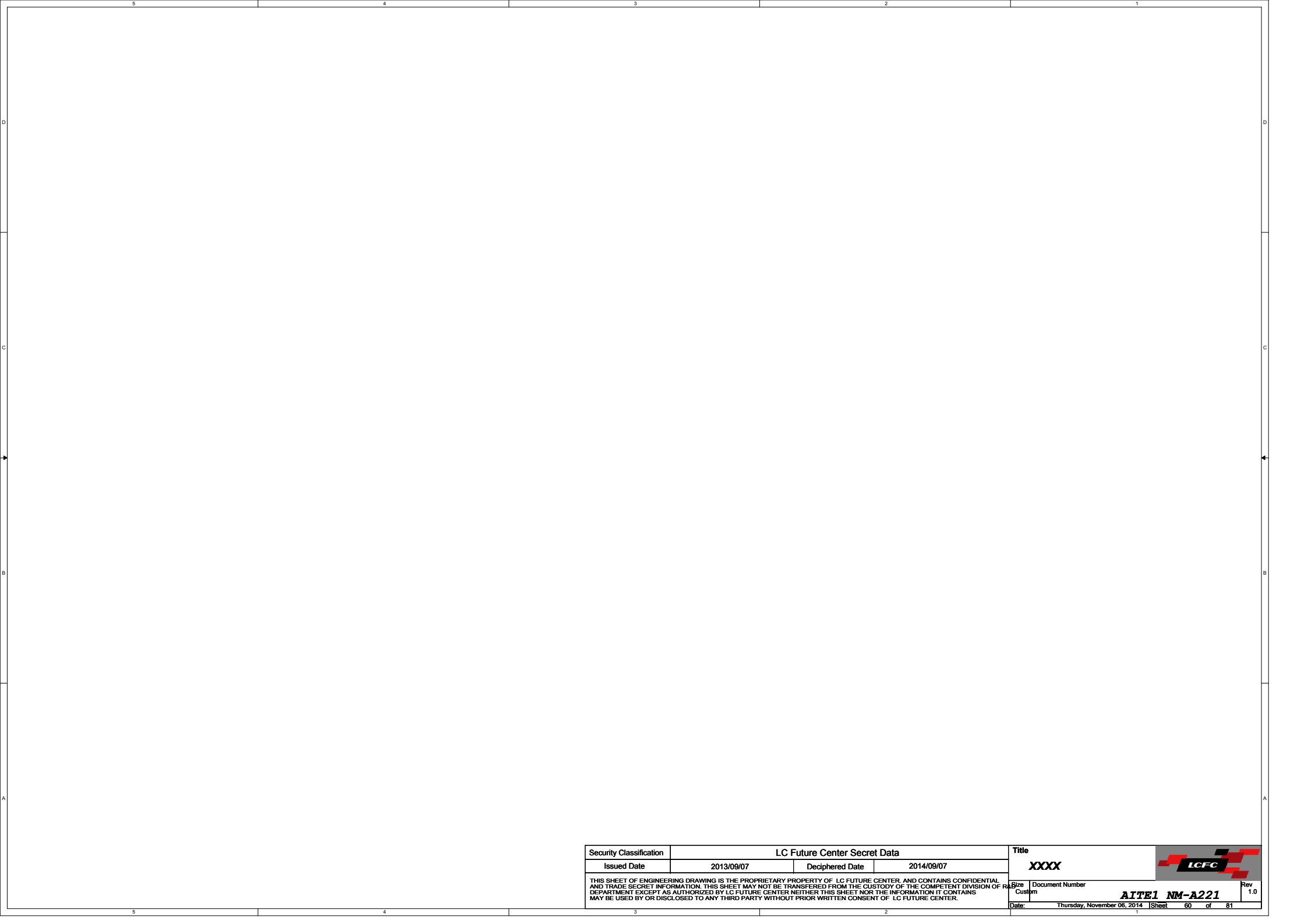
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+3VALW To +3V_PCH

80 mils

0.271 A

80 mils

0.271 A

0.0805_5%

J7

1 2

3

Q6

AO3413_SOT23-3

R7

10K_0402_5%

R96

100K_0402_5%

C68

4.7U_0603_10V6-K

C66

0.1U_0402_16V7-K

PCH_PWR_EN#

PCH_PWR_EN#

If support Deep and Mirror,
R96 need to set MIRROR@

+3VALW

+3V_PCH

The schematic diagram illustrates the +5V_DDR voltage divider circuit. It features a voltage divider network with a 10k resistor (R23) and a 100k resistor (C43) connected to the +5VALW supply. The output of the divider is connected to the IN2 pin of the voltage detector U7 (GS243AT11U). The IN1 pin of U7 is connected to GND. The OUT pin of U7 is connected to the +5V_DDR supply. The EN pin of U7 is connected to the SYSON signal. The circuit is powered by +5VALW and +5V_DDR.

+3VALW to +3VM


If support SBA and Mirror,
R228 need to set MIRROR@

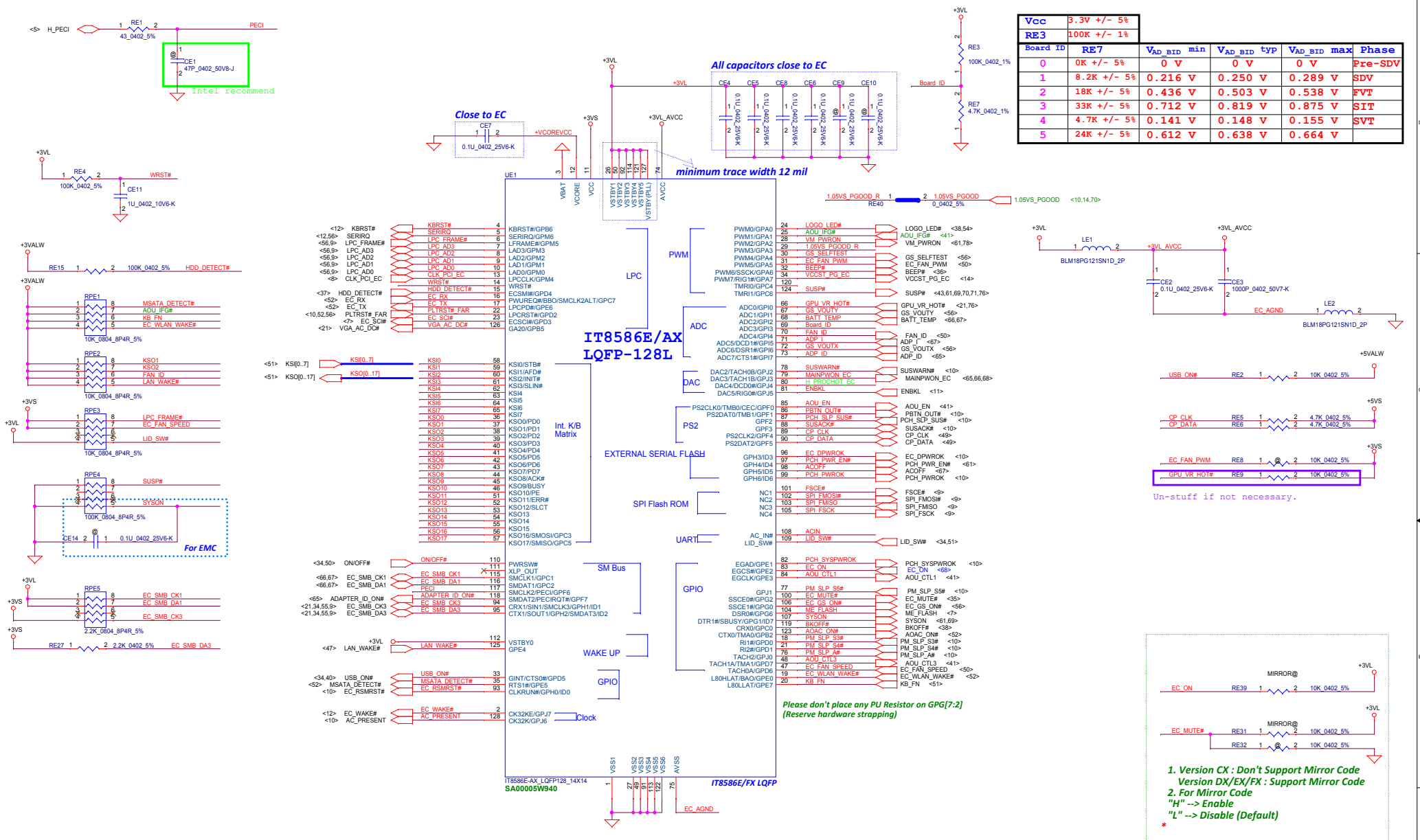
<62,78> VM_PWRON

VM_PWRON

VM_PWRON#

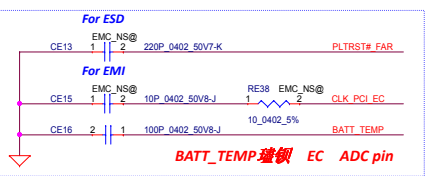
For SPI ROM/LAN VPRO

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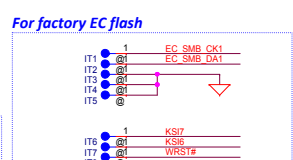
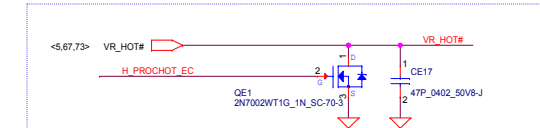


Vcc	3.3V +/- 5%				
RE3	100K +/- 1%				
Board ID	RE7	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	Pre-SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SVT
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

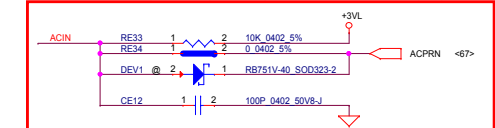
1. Version CX : Don't Support Mirror Code
Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
*



PROCHOT#
(EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)



AC IN, need to confirm the pin is High or Low active while pulg ACIN

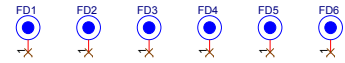


Screw Hole




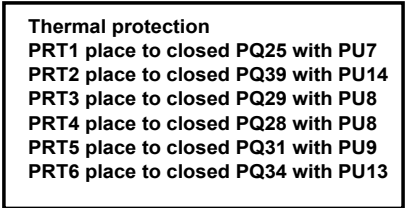
Center Zero

PCB Fedical Mark PAD

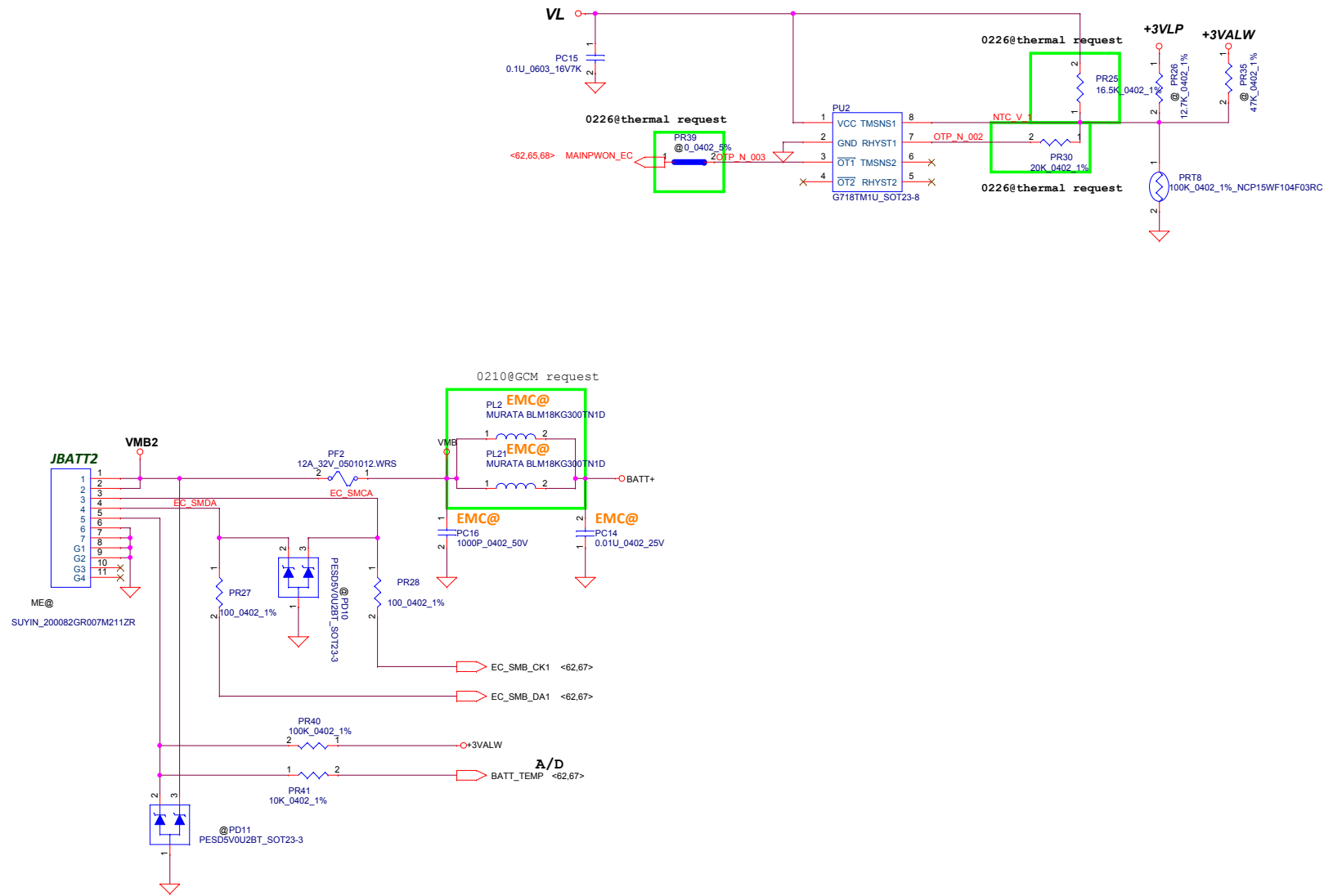


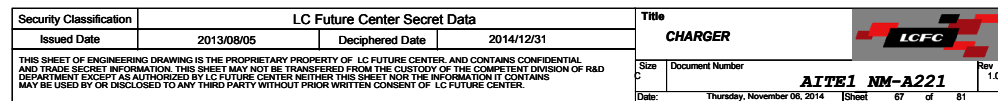
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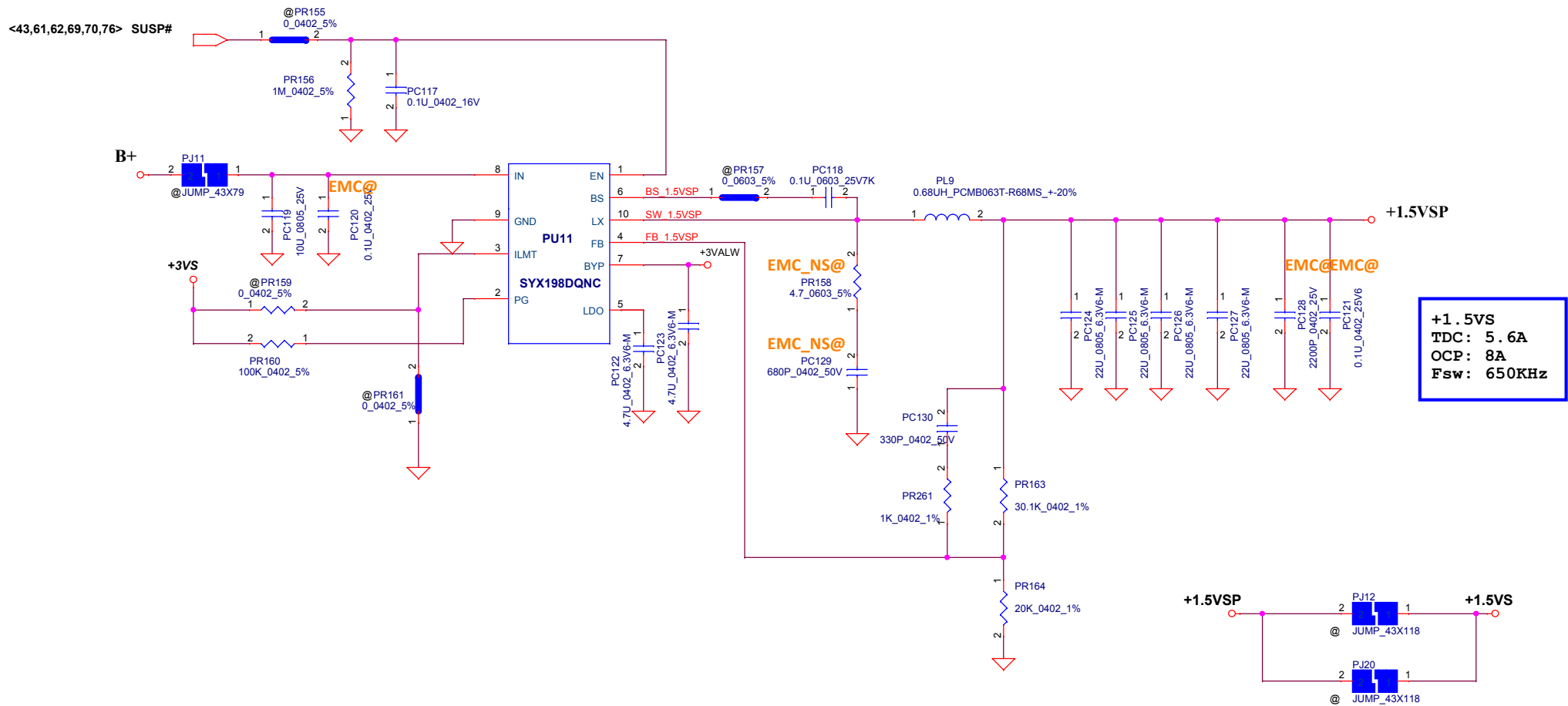
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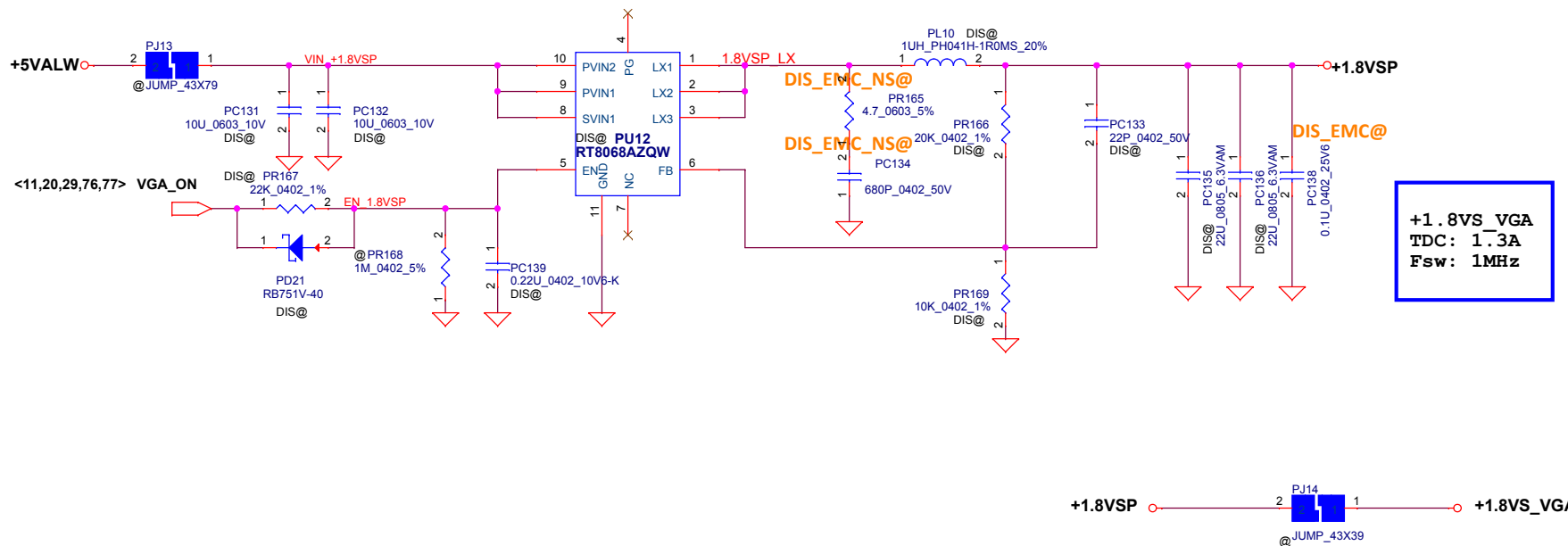
PRT8 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C




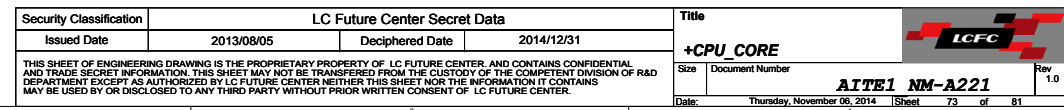




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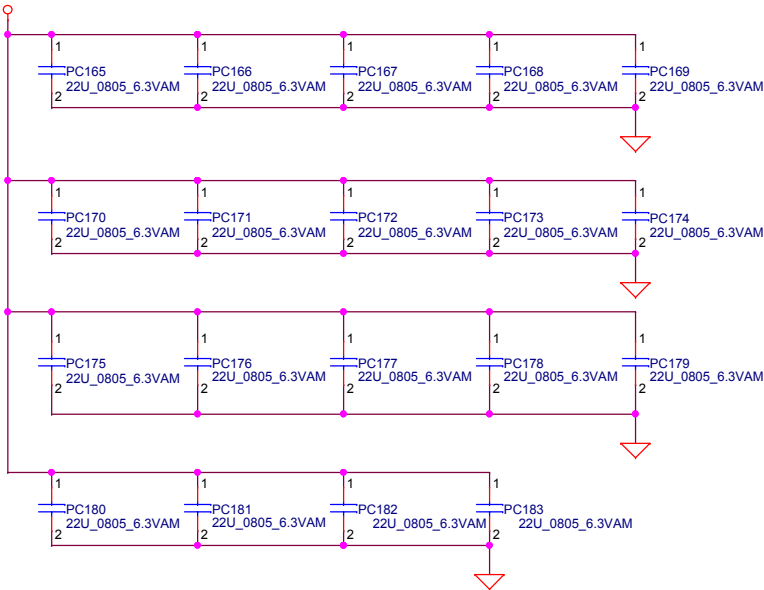



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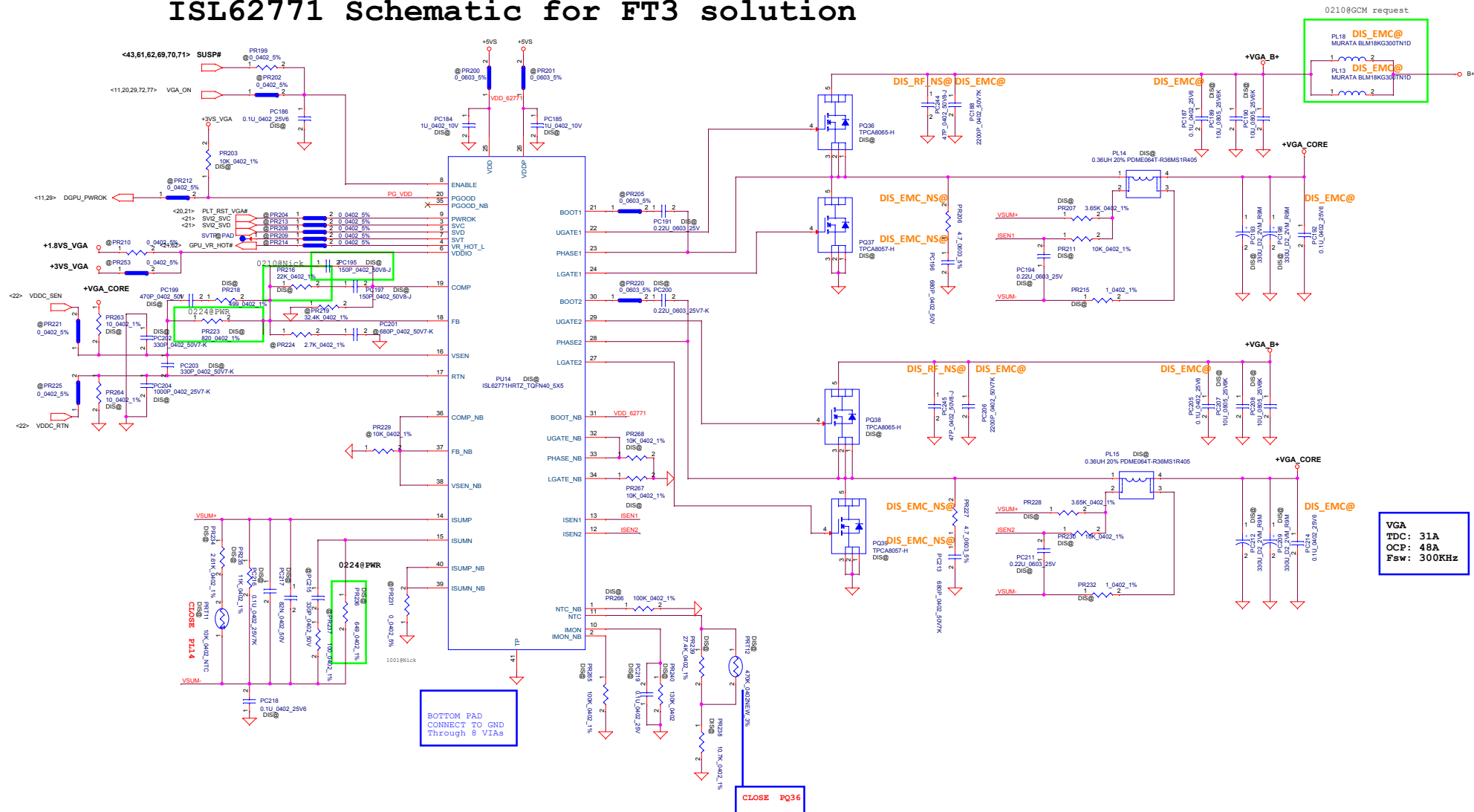
Based on PDDG rev 0.7 Table 5-1.


+VCC_CORE



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ISL62771 Schematic for FT3 solution

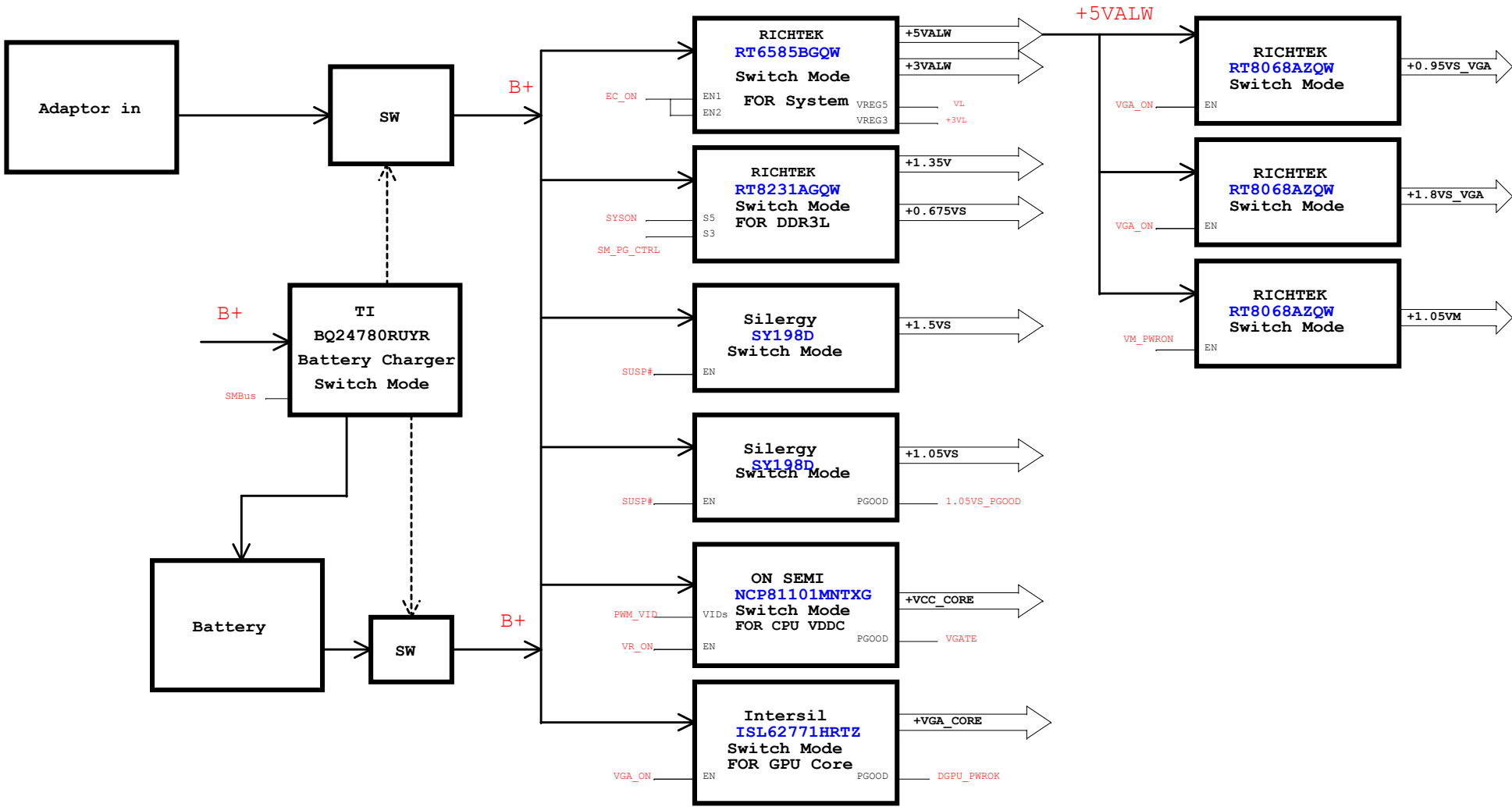


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<p>ATTEI NM-A221</p>					

POWER PIR (Product Improve Record)

AITE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16


NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
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HW PIR (Product Improve Record)

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Gordon SDV LOGIC SCHEMATICS

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Nov/13/2013

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2.BLOCK DIAGRAM
3.NOTE LIST
4.VGA NOTE
5.BDW_DDI/EDP/XDP
6.BDW_DDR3L INT
7.BDW_RTC/HDA/SATA/PCIe/JTAG
8.BDW_CLOCK/PM
9.BDW_LPC/SPI/SM BUS
10.BDW_SYS PM
11.BDW_eDP SBAND/DDPx
12.BDW_GPIO/SIO
13.BDW_PCIE/USB BUS
14.BDW (Power)
15.BDW (Power2)
16.BDW (VSS)
17.BDW (OTHER)
18.DDR3L DIMM1
19.DDR3L DIMM2
20.Opal & Jet PCIE
21.Opal & Jet GPIO
22.Opal & Jet Core Power
23.Opal & Jet DP Power/GND
24.Opal & Jet MEM Interface
25.Opal & Jet DDR3 VRAM U
26.Opal & Jet DDR3 VRAM L
27.Opal 22 TO 24 VRAM U2
28.Opal 23 TO 25 VRAM L2
29.Opal & Jet swich power
30.BLANK
31.BLANK
32.CARDREADER IC/CONN.
33.DP RP --> BLANK
34.DOCKING/ DCIN CONN
35.CX20751

36.HP/MIC JACK/Speaker
37.SATA HDD/ODD CONN.
38.eDP/CMOS CONN.
39.USB30 RP --> BLANK
40.USB3 PORT1-BACK
41.USB3 PORT2-FRONT(AOU)
42.MUX IC
43.DP TO VGA
44.VGA CONN.
45.HDMI RP --> BLANK
46.HDMI CONN.
47.GBE LAN PHY
48.RJ45 CONN.
49.CP/TPOINTCONN.
50.PBTN/LID/FP/FAN CONN.
51.KB/RTC/TOUCH PAN CONN.
52.WWAN/WLAN NGFF CONN.
53.SUB CONN. --> BLANK
54.SUB-AUDIO JACK CONN.
55.THERMAL SENSOR
56.G SENSOR/TPM
57.BLANK
58.BLANK
59.BLANK
60.BLANK
61.DC V TO VS/ V-PCH/VM
62.EC_IT8586E/FX
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65.DCIN / Vin Detector
66.BATTERY CONN/OTP
67.CHARGER(BQ24780)
68.3V/5VALW(RT6585B)
69.+1.35V/+0.675V(RT8231A)
70.+1.05VS(SYX198DQNC)

71.+1.5VS(SYX198DQNC)
72.+1.8VS_VGA(RT8068A)
73.+VCC_CORE(NCP81101MNTXG)
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77.+0.95VS_VGA(RT8068A)
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80.HW PIR

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